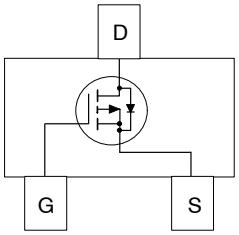
MOSFET – Single P-Channel POWERTRENCH®

2.5 V Specified

FDN336P

SOT−23
CASE 527AG



Description

This P−Channel 2.5 V specified MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been especially tailored to minimize the on−state resistance and yet maintain low gate charge for superior switching performance.

These devices are well suited for portable electronics applications: load switching and power management, battery charging circuits and DC−DC conversion.

Features

- −1.3 A, −20 V
  - $R_{DS(on)}$ = 0.20 Ω @ V_{GS} = −4.5 V
  - $R_{DS(on)}$ = 0.27 Ω @ V_{GS} = −2.5 V
- Low Gate Charge (3.6 nC Typical)
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- SUPERSOT^{TM} −3 Provides Low $R_{DS(ON)}$ and 30% Higher Power Handling Capability than SOT23 in the Same Footprint

MARKING DIAGRAM

336 = Specific Device Code
M = Month Code
▪ = Pb−Free Package

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	−20	V
V_{GSS}	Gate to Source Voltage	±8	V
I_D	Drain Current − Continuous (Note 1a) − Pulsed	 −1.3 −10	A
P_D	Maximum Power Dissipation (Note 1a) (Note 1b)	 0.5 0.46	W
T_J, T_{stg}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

Device	Package	Shipping†
FDN336P	SOT−23 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 1a)	250	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction−to−Case (Note 1)	75	°C/W

ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = −250 μA	−20	−	−	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = −250 μA, Referenced to 25°C	−	−16	−	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −16 V, V_{GS} = 0 V	−	−	−1	μA
		V_{DS} = −16 V, V_{GS} = 0 V, T_J = 55°C	−	−	−10	μA
I_{GSSF}	Gate−Body Leakage Forward	V_{GS} = 8 V, V_{DS} = 0 V	−	−	100	nA
I_{GSSR}	Gate−Body Leakage Reverse	V_{GS} = −8 V, V_{DS} = 0 V	−	−	−100	nA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = −250 μA	−0.4	−0.9	−1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = −250 μA, Referenced to 25°C	−	3	−	mV/°C
$R_{DS(on)}$	Static Drain−Source On−Resistance	V_{GS} = −4.5 V, I_D = −1.3 A V_{GS} = −4.5 V, I_D = −1.3 A, T_J = 125°C V_{GS} = −2.5 V, I_D = −1.1 A	− − −	0.122 0.18 0.19	0.2 0.32 0.27	Ω
$I_{D(on)}$	On−State Drain Current	V_{GS} = −4.5 V, V_{DS} = −5 V	−5	−	−	A
g_{FS}	Forward Transconductance	V_{DS} = −4.5 V, I_D = −2 A		4	−	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = −10 V, V_{GS} = 0 V, f = 1.0 MHz	−	330	−	pF
C_{oss}	Output Capacitance		−	80	−	pF
C_{rss}	Reverse Transfer Capacitance		−	35	−	pF
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = −5 V, I_D = −0.5 A, V_{GS} = −4.5 V, R_{GEN} = 6 Ω	−	7	15	ns
t_r	Turn−On Rise Time		−	12	22	ns
$t_{d(off)}$	Turn−Off Delay Time		−	16	26	ns
t_f	Turn−Off Fall Time		−	5	12	ns
Q_g	Total Gate Change	V_{DS} = −10 V, I_D = −2 A, V_{GS} = −4.5 V	−	3.6	5	nC
Q_{gs}	Gate−Source Change		−	0.8	−	nC
Q_{gd}	Gate−Drain Change		−	0.7	−	nC
Drain−Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain−Source Diode Forward Current		−	−	−0.42	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = −0.42 A (Note 2)	−	−0.7	−1.2	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 250°C/W when mounted on a 0.02 in² Pad of 2 oz. Cu.

b) 270°C/W on a minimum mounting pad of 2 oz. Cu.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%

TYPICAL CHARACTERISTICS

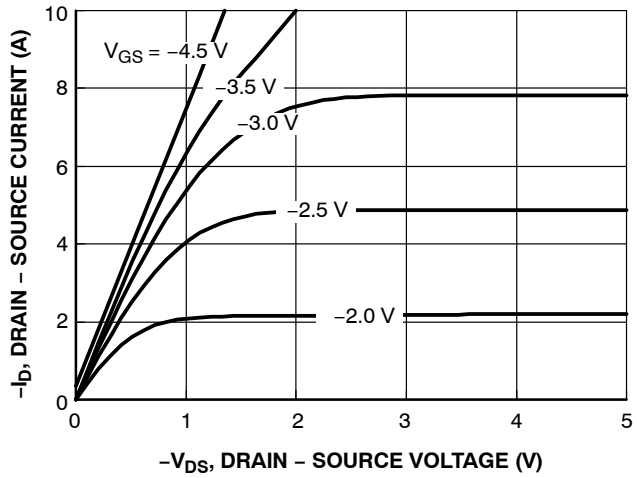


Figure 1. On−Region Characteristics

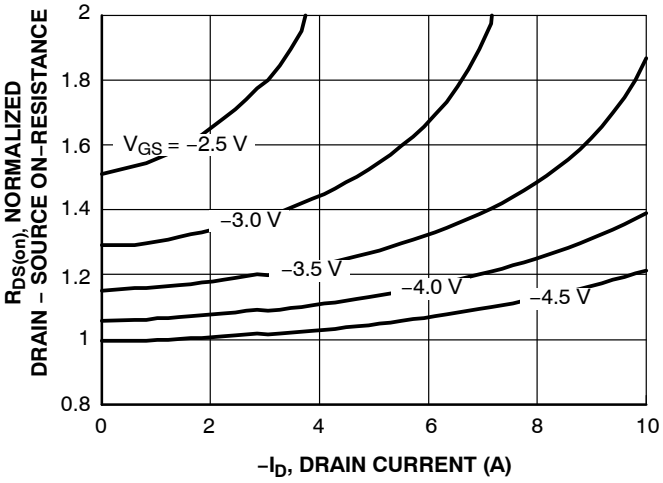


Figure 2. On−Resistance Variation with Drain Current and Gate

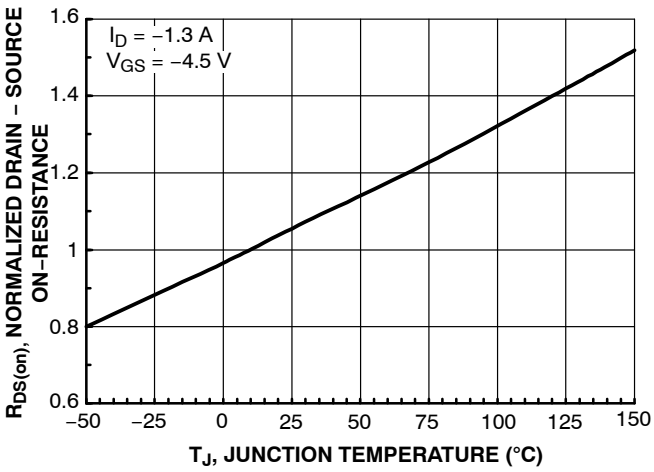


Figure 3. On−Resistance Variation with Temperature

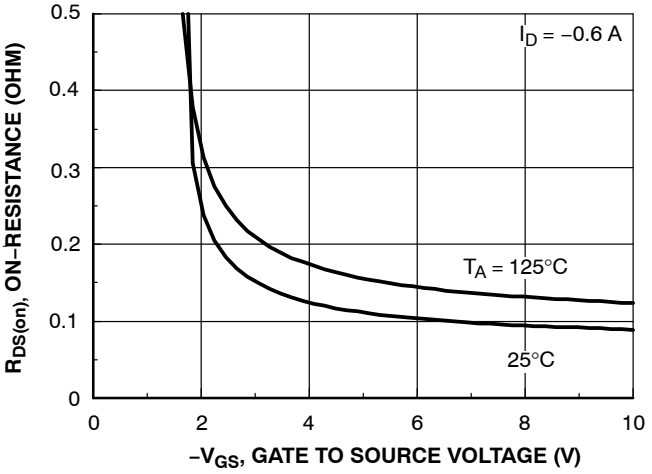


Figure 4. On−Resistance Variation with Gate−to−Source Voltage

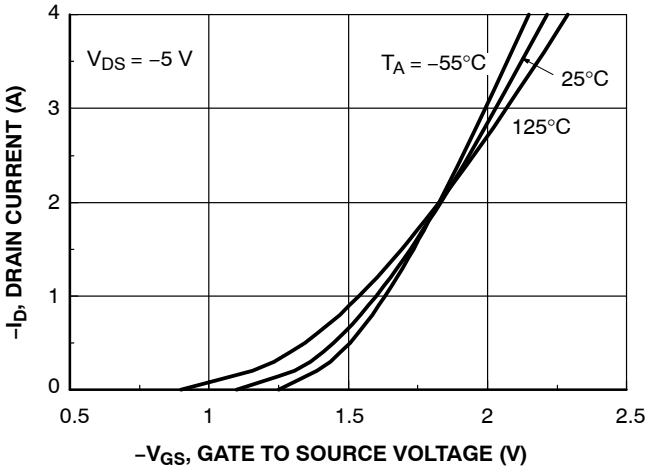


Figure 5. Transfer Characteristics

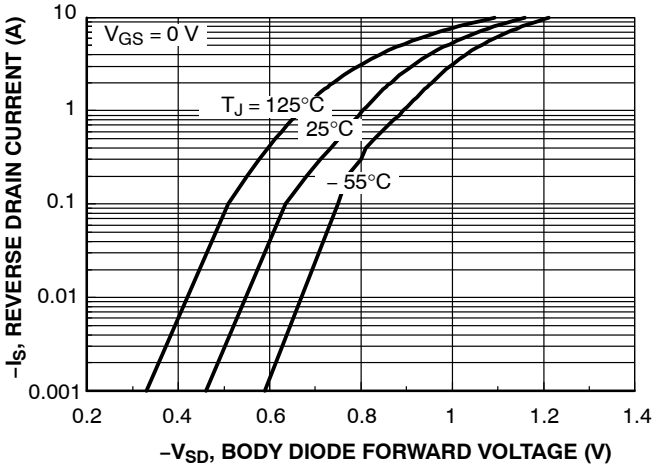


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (CONTINUED)

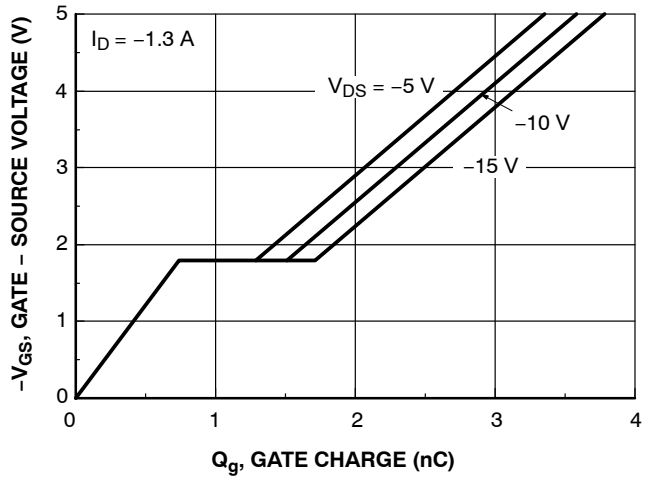


Figure 7. Gate Charge Characteristics

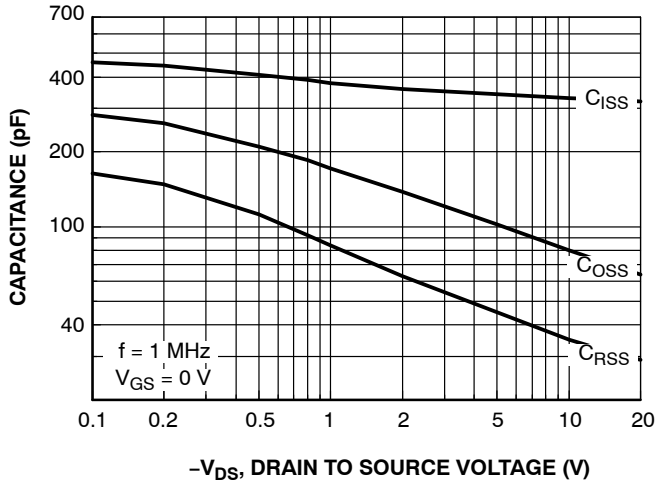


Figure 8. Capacitance Characteristics

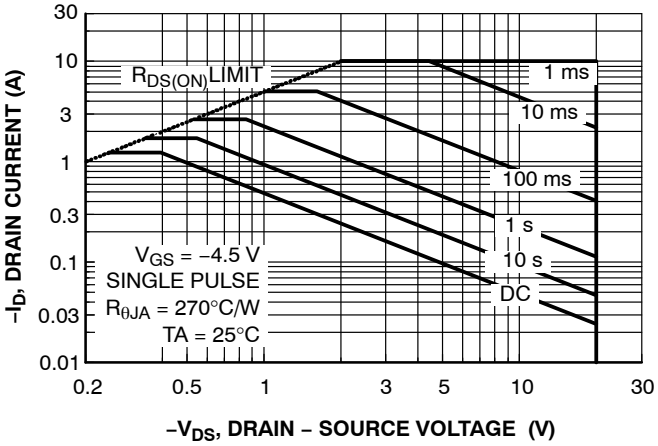


Figure 9. Maximum Safe Operating Area

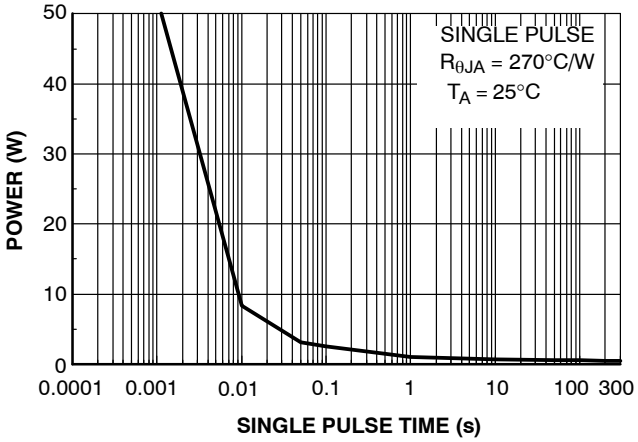


Figure 10. Single Pulse Maximum Power Dissipation

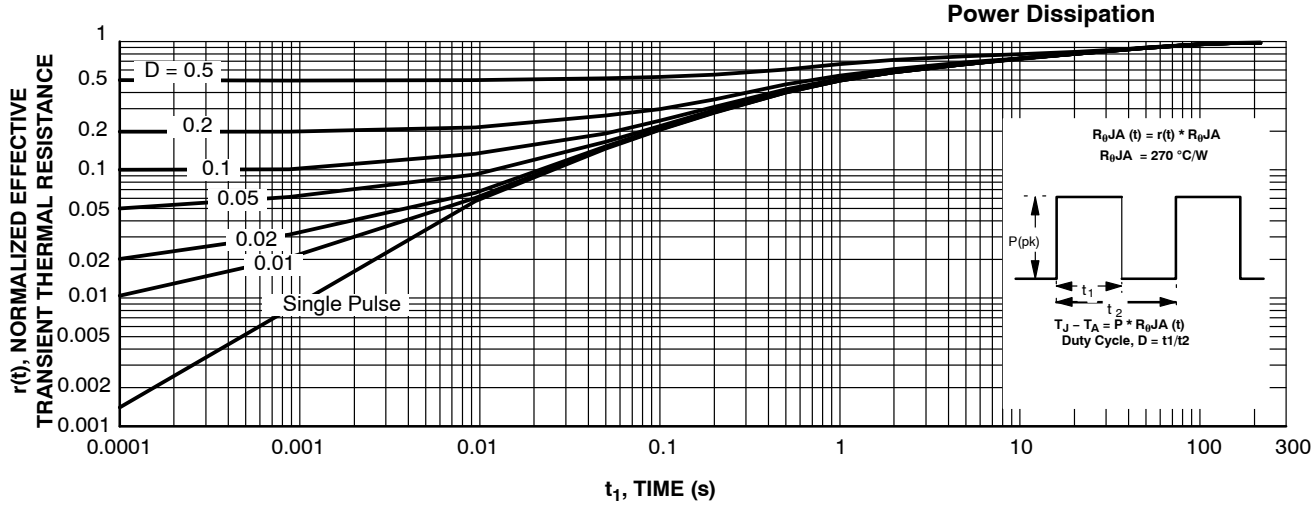
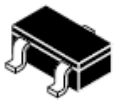


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note 1b.
Transient themal response will change depending on the circuit board design.

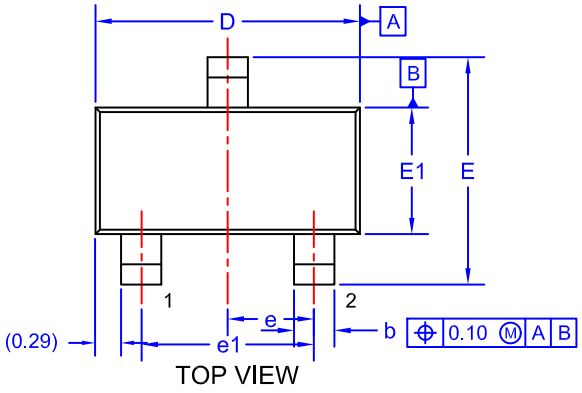
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



SOT−23/SUPERSOT™ −23, 3 LEAD, 1.4x2.9
CASE 527AG
ISSUE A

DATE 09 DEC 2019

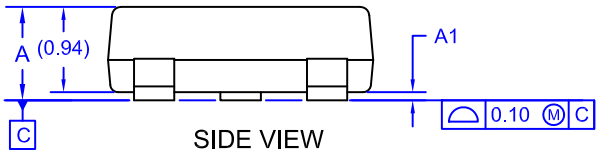


TOP VIEW

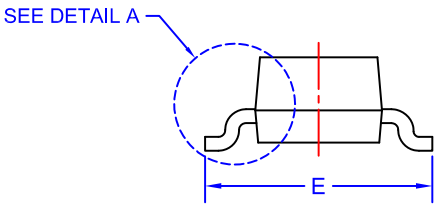
NOTES: UNLESS OTHERWISE SPECIFIED

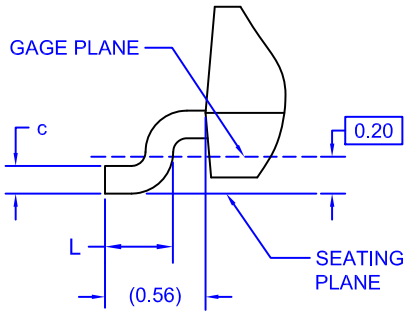
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

DIM	MIN.	NOM.	MAX.
A	0.85	0.95	1.12
A1	0.00	0.05	0.10
b	0.370	0.435	0.508
c	0.085	0.150	0.180
D	2.80	2.92	3.04
E	2.31	2.51	2.71
E1	1.20	1.40	1.52
e		0.95 BSC	
e1		1.90 BSC	
L	0.33	0.38	0.43

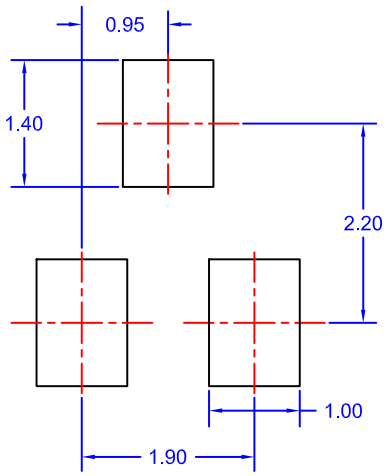


SIDE VIEW





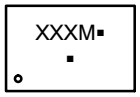
DETAIL A



LAND PATTERN RECOMMENDATION*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Month Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**SOT−23/SUPERSOT−23, 3 LEAD, 1.4X2.9**	**PAGE 1 OF 1**

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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For additional information, please contact your local Sales Representative

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