

## TOSHIBA Memory e-MMC Module

16GB THGAMRG7T13BAIL

### INTRODUCTION

THGAMRG7T13BAIL is 16GB density of e-MMC Module product housed in 153 ball BGA package. This unit is utilized advanced TOSHIBA NAND flash device(s) and controller chip assembled as Multi Chip Module. THGAMRG7T13BAIL has an industry standard MMC protocol for easy use.

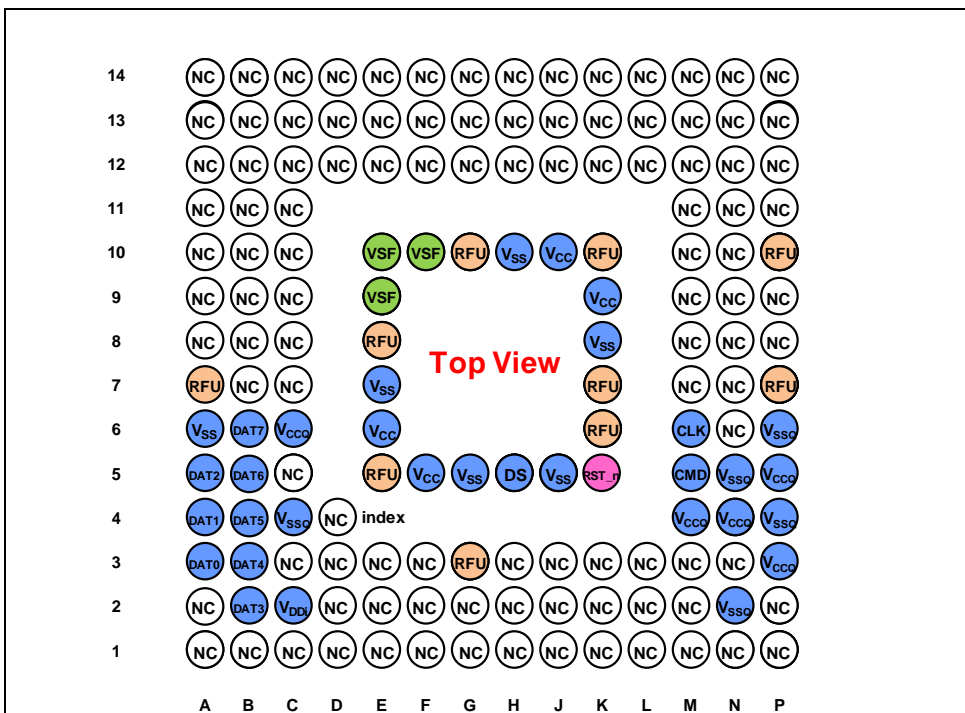
### FEATURES

#### THGAMRG7T13BAIL Interface

THGAMRG7T13BAIL has the JEDEC/MMCA Version 5.1 interface with 1-I/O, 4-I/O and 8-I/O mode.

#### Pin Connection

P-WFBGA153-1113-0.50 (11.5mm x 13mm, H0.8mm max. package)



Pin Number	Name	Pin Number	Name	Pin Number	Name	Pin Number	Name
A3	DAT0	C2	V <sub>DDi</sub>	J5	V <sub>SS</sub>	N4	V <sub>CCQ</sub>
A4	DAT1	C4	V <sub>SSQ</sub>	J10	V <sub>CC</sub>	N5	V <sub>SSQ</sub>
A5	DAT2	C6	V <sub>CCQ</sub>	K5	RST <sub>n</sub>	P3	V <sub>CCQ</sub>
A6	V <sub>SS</sub>	E6	V <sub>CC</sub>	K8	V <sub>SS</sub>	P4	V <sub>SSQ</sub>
B2	DAT3	E7	V <sub>SS</sub>	K9	V <sub>CC</sub>	P5	V <sub>CCQ</sub>
B3	DAT4	F5	V <sub>CC</sub>	M4	V <sub>CCQ</sub>	P6	V <sub>SSQ</sub>
B4	DAT5	G5	V <sub>SS</sub>	M5	CMD		
B5	DAT6	H5	DS	M6	CLK		
B6	DAT7	H10	V <sub>SS</sub>	N2	V <sub>SSQ</sub>		

NC: No Connect, shall be connected to ground or left floating.

RFU: Reserved for Future Use, shall be left floating for future use.

VSF: Vendor Specific Function, shall be left floating.

## Part Number

### Available e-MMC Module Product – Part Number

Part Number	Density	Package Size	NAND Flash Type	Weight
THGAMRG7T13BAIL	16GB	11.5mm x 13mm x 0.8mm(max)	1 x 128Gbit BiCS3	TBD typ.

## Temperature

Characteristics	Min	Max	Unit
Operating temperature	-25	85	°C
Storage temperature	-40	85	°C

Note: Avoid locations where e-MMC devices may be exposed to water (wet, rain, dew condensation, etc).

## Performance

X8 mode/ Sequential access(4MByte access size)

Part Number	Density	NAND Flash Type	Interleave Operation	Frequency /Mode	V <sub>CCQ</sub>	Typ. Performance [MB/s]	
						Read	Write
THGAMRG7T13BAIL	16GB	1 x 128Gbit BiCS3	Non Interleave	52MHz/SDR	1.8V	45	TBD
				52MHz/DDR	1.8V	85	TBD
				HS200	1.8V	175	TBD
				HS400	1.8V	310	110

## Power Supply

V<sub>CC</sub> = 2.7V to 3.6V

V<sub>CCQ</sub> = 1.7V to 1.95V

## Operating Current (RMS)

The measurement for max RMS current is done as average RMS current consumption over a period of 100ms.

Part Number	Density	NAND Flash Type	Interleave Operation	Frequency /Mode	V <sub>CCQ</sub>	Max Operating Current [mA]	
						I <sub>CCQ</sub>	I <sub>CC</sub>
THGAMRG7T13BAIL	16GB	1 x 128Gbit BiCS3	Non Interleave	52MHz/SDR	1.8V	TBD	TBD
				52MHz/DDR	1.8V	TBD	TBD
				HS200	1.8V	TBD	TBD
				HS400	1.8V	TBD	TBD

**Sleep Mode Current**

Part Number	Density	NAND Flash Type	Interleave Operation	I <sub>CCQs</sub> [μA]		I <sub>CCQs</sub> +I <sub>CCS</sub> [μA]	
				Typ. <sup>Note 1</sup>	Max. <sup>Note 2</sup>	Typ. <sup>Note 1</sup>	Max. <sup>Note 2</sup>
THGAMRG7T13BAIL	16GB	1 x 128Gbit BiCS3	Non Interleave	TBD	TBD	TBD	TBD

Note 1: The conditions of typical values are 25°C and V<sub>CCQ</sub> = 1.8V.

Note 2: The conditions of maximum values are 85°C and V<sub>CCQ</sub> = 1.95V.

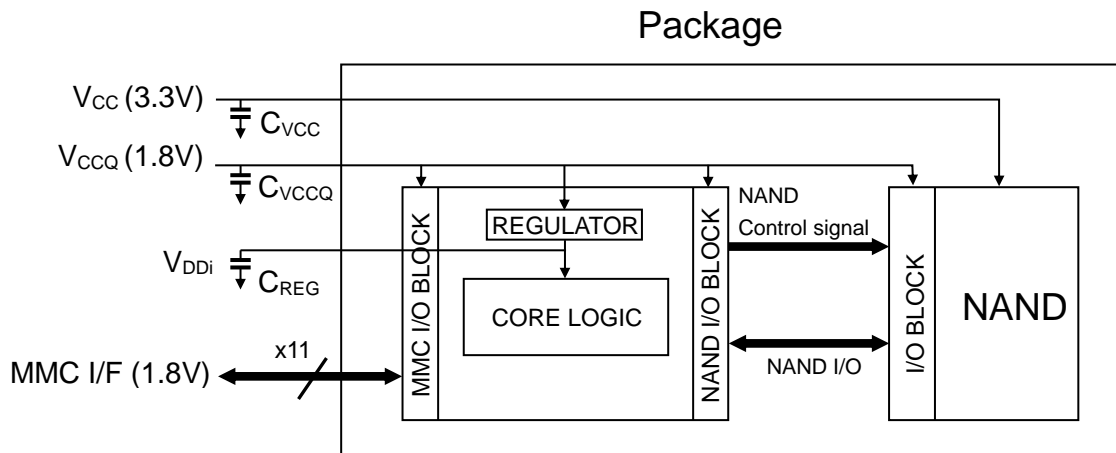
**Product Architecture**

The diagram in Figure 1 illustrates the main functional blocks of the THGAMRG7T13BAIL.

Specification of the C<sub>REG</sub> and recommended values of the C<sub>VCC</sub>, and C<sub>VCCQ</sub> in the Figure 1 are as follows.

Parameter	Symbol	Unit	Min.	Typ.	Max.	Remark
V <sub>DDi</sub> capacitor value	C <sub>REG</sub>	μF	1	2.2 <sup>Note 1</sup>	4.7	
V <sub>CC</sub> capacitor value	C <sub>VCC</sub>	μF	-	4.7 + 0.22	-	
V <sub>CCQ</sub> capacitor value	C <sub>VCCQ</sub>	μF	-	4.7 + 0.1	-	

Note 1: Toshiba Memory recommends that the value should be usually applied as the value of C<sub>REG</sub>.



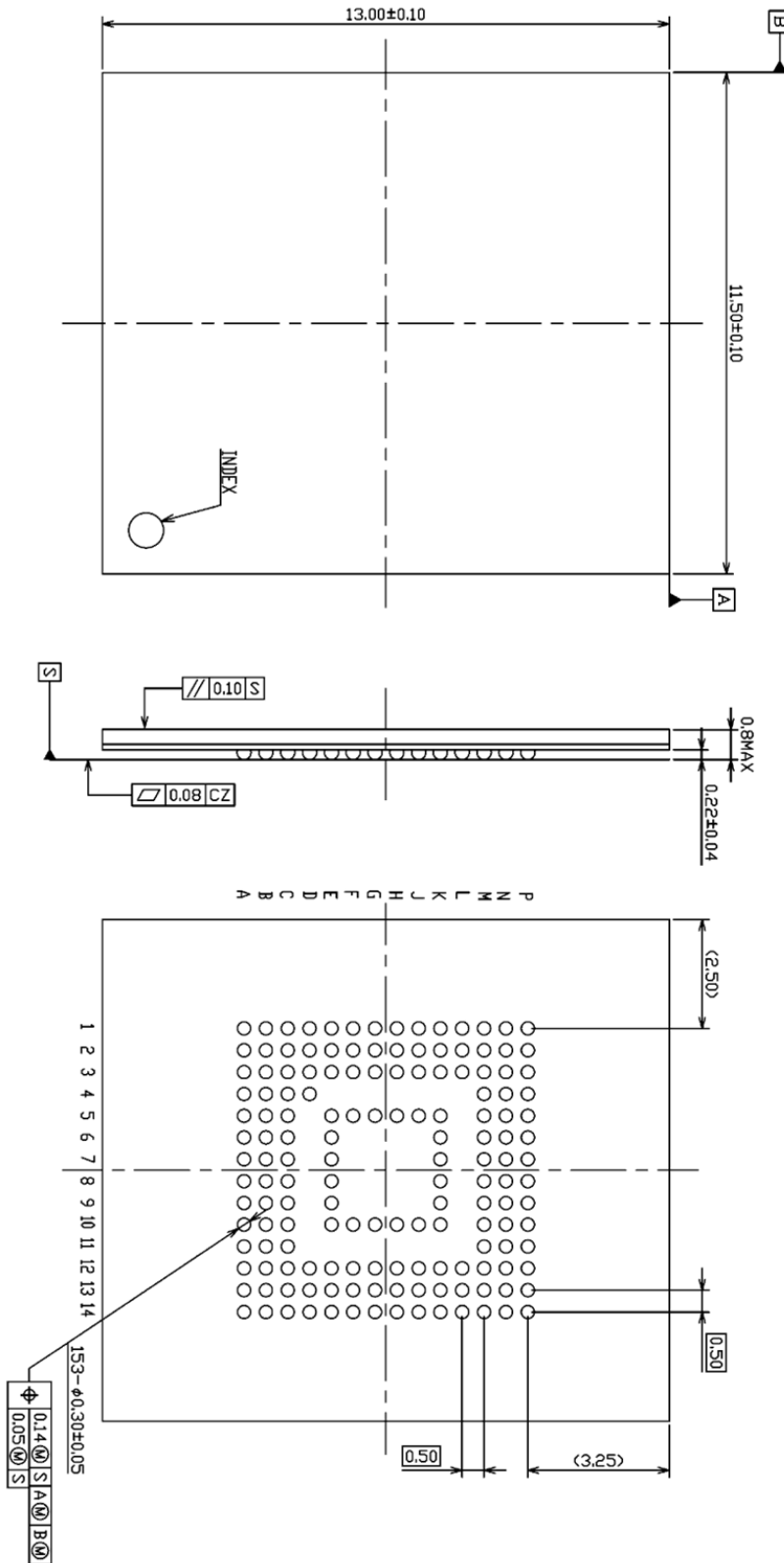
**Figure 1 THGAMRG7T13BAIL Block Diagram**

**PRODUCT SPECIFICATIONS**

**Package Dimensions**

P-WFBGA153-1113-0.50 (11.5mm x 13mm, H0.8mm max. package)

Unit: mm



**Density Specifications**

Density	Part Number	Interleave Operation	User Area Density [Bytes]	SEC_COUNT in Extended CSD
16GB	THGAMRG7T13BAIL	Non Interleave	15,552,479,232	0x01CF8000

Note: User area density shall be reduced if enhanced user data area is defined.

**Register Informations**

**OCR Register**

OCR bit	VDD Voltage window	Value
[6:0]	Reserved	000 0000b
[7]	1.70-1.95 V	1b
[14:8]	2.0-2.6 V	000 0000b
[23:15]	2.7-3.6 V	1 1111 1111b
[28:24]	Reserved	0 0000b
[30:29]	Access Mode	10b
[31]	( card power up status bit (busy) ) <sup>Note</sup>	

Note: This bit is set to LOW if the Device has not finished the power up routine.

**CID Register**

CID-slice	Name	Field	Width	Value
[127:120]	Manufacturer ID	MID	8	0001 0001b
[119:114]	Reserved	-	6	0b
[113:112]	Device/BGA	CBX	2	01b
[111:104]	OEM/Application ID	OID	8	0b
[103:56]	Product name	PNM	48	0x30 31 36 47 30 30 (016G00)
[55:48]	Product revision	PRV	8	0x00
[47:16]	Product serial	PSN	32	Serial number
[15:8]	Manufacturing date	MDT	8	see-JEDEC Specification
[7:1]	CRC7 checksum	CRC	7	CRC7
[0]	Not used, always '1'	-	1	1b

### CSD Register

CSD-slice	Name	Field	Width	Cell Type	Value
[127:126]	CSD structure	CSD_STRUCTURE	2	R	0x3
[125:122]	System specification version	SPEC_VERS	4	R	0x4
[121:120]	Reserved	-	2	R	0x0
[119:112]	Data read access-time 1	TAAC	8	R	0x4F
[111:104]	Data read access-time 2 in CLK cycles (NSAC * 100)	NSAC	8	R	0x0
[103:96]	Max. bus clock frequency	TRAN_SPEED	8	R	0x32
[95:84]	Device command classes	CCC	12	R	0x8F5
[83:80]	Max. read data block length	READ_BL_LEN	4	R	0x9
[79:79]	Partial blocks for read allowed	READ_BL_PARTIAL	1	R	0x0
[78:78]	Write block misalignment	WRITE_BLK_MISALIGN	1	R	0x0
[77:77]	Read block misalignment	READ_BLK_MISALIGN	1	R	0x0
[76:76]	DSR implemented	DSR_IMP	1	R	0x0
[75:74]	Reserved	-	2	R	0x0
[73:62]	Device size	C_SIZE	12	R	0xFFF
[61:59]	Max. read current @ VDD min.	VDD_R_CURR_MIN	3	R	0x7
[58:56]	Max. read current @ VDD max.	VDD_R_CURR_MAX	3	R	0x7
[55:53]	Max. write current @ VDD min.	VDD_W_CURR_MIN	3	R	0x7
[52:50]	Max. write current @ VDD max.	VDD_W_CURR_MAX	3	R	0x7
[49:47]	Device size multiplier	C_SIZE_MULT	3	R	0x7
[46:42]	Erase group size	ERASE_GRP_SIZE	5	R	0x1F
[41:37]	Erase group size multiplier	ERASE_GRP_MULT	5	R	0x1F
[36:32]	Write protect group size	WP_GRP_SIZE	5	R	0x0F
[31:31]	Write protect group enable	WP_GRP_ENABLE	1	R	0x1
[30:29]	Manufacturer default ECC	DEFAULT_ECC	2	R	0x0
[28:26]	Write speed factor	R2W_FACTOR	3	R	0x2
[25:22]	Max. write data block length	WRITE_BL_LEN	4	R	0x9
[21:21]	Partial blocks for write allowed	WRITE_BL_PARTIAL	1	R	0x0
[20:17]	Reserved	-	4	R	0x0
[16:16]	Content protection application	CONTENT_PROT_APP	1	R	0x0
[15:15]	File format group	FILE_FORMAT_GRP	1	R/W	0x0
[14:14]	Copy flag (OTP)	COPY	1	R/W	0x0
[13:13]	Permanent write protection	PERM_WRITE_PROTECT	1	R/W	0x0
[12:12]	Temporary write protection	TMP_WRITE_PROTECT	1	R/W/E	0x0
[11:10]	File format	FILE_FORMAT	2	R/W	0x0
[9:8]	ECC code	ECC	2	R/W/E	0x0
[7:1]	CRC	CRC	7	R/W/E	CRC
[0]	Not used, always '1'	-	1	-	0x1

### Extended CSD Register

CSD-slice	Name	Field	Size (Bytes)	Cell Type	Value
[511:506]	Reserved	-	6	-	All '0'
[505]	Extended Security Commands Error	EXT_SECURITY_ERR	1	R	0x00
[504]	Supported Command Sets	S_CMD_SET	1	R	0x01
[503]	HPI features	HPI_FEATURES	1	R	0x01
[502]	Background operations support	BKOPS_SUPPORT	1	R	0x01
[501]	Max_packed read commands	MAX_PACKED_READS	1	R	0x3C
[500]	Max_packed write commands	MAX_PACKED_WRITES	1	R	0x20
[499]	Data Tag Support	DATA_TAG_SUPPORT	1	R	0x01
[498]	Tag Unit Size	TAG_UNIT_SIZE	1	R	0x03
[497]	Tag Resource Size	TAG_RES_SIZE	1	R	0x00
[496]	Context management capabilities	CONTEXT_CAPABILITIES	1	R	0x05
[495]	Large Unit size	LARGE_UNIT_SIZE_M1	1	R	0x17
[494]	Extended partitions attribute support	EXT_SUPPORT	1	R	0x03
[493]	Supported modes	SUPPORTED_MODES	1	R	0x01
[492]	FFU features	FFU_FEATURES	1	R	0x00
[491]	Operation codes timeout	OPERATION_CODES_TIMEOUT	1	R	0x00
[490:487]	FFU Argument	FFU_ARG	4	R	0xFFFFFFFF
[486]	Barrier support	BARRIER_SUPPORT	1	R	0x01
[485:309]	Reserved	-	177	-	All '0'
[308]	CMD Queuing Support	CMDQ_SUPPORT	1	R	0x01
[307]	CMD Queuing Depth	CMDQ_DEPTH	1	R	0x1F
[306]	Reserved	-	1	-	0x00
[305:302]	Number of FW sectors correctly programmed	NUMBER_OF_FW_SECTORS_CORRECTLY_PROGRAMMED	4	R	All '0'
[301:270]	Vendor proprietary health report	VENDOR_PROPRIETARY_HEALTH_REPORT	32	R	All '0'
[269]	Device life time estimation type B	DEVICE_LIFE_TIME_EST_TYP_B	1	R	0x01
[268]	Device life time estimation type A	DEVICE_LIFE_TIME_EST_TYP_A	1	R	0x01
[267]	Pre EOL information	PRE_EOL_INFO	1	R	0x01
[266]	Optimal read size	OPTIMAL_READ_SIZE	1	R	0x01
[265]	Optimal write size	OPTIMAL_WRITE_SIZE	1	R	0x08
[264]	Optimal trim unit size	OPTIMAL_TRIM_UNIT_SIZE	1	R	0x01
[263:262]	Device version	DEVICE_VERSION	2	R	0x00
[261:254]	Firmware version	FIRMWARE_VERSION	8	R	0x01
[253]	Power class for 200MHz, DDR at V <sub>CC</sub> =3.6V	PWR_CL_DDR_200_360	1	R	0x00
[252:249]	Cache size	CACHE_SIZE	4	R	0x00000400
[248]	Generic CMD6 timeout	GENERIC_CMD6_TIME	1	R	0x32
[247]	Power off notification(long) timeout	POWER_OFF_LONG_TIME	1	R	0x40
[246]	Background operations status	BKOPS_STATUS	1	R	0x00
[245:242]	Number of correctly programmed sectors	CORRECTLY_PRG_SECTORS_NUM	4	R	0x00000000
[241]	1 <sup>st</sup> initialization time after partitioning	INI_TIMEOUT_AP	1	R	0x64

CSD-slice	Name	Field	Size (Bytes)	Cell Type	Value
[240]	Cache Flushing Policy	CACHE_FLUSH_POLICY	1	R	0x01
[239]	Power class for 52MHz, DDR at 3.6V	PWR_CL_DDR_52_360	1	R	0x00
[238]	Power class for 52MHz, DDR at 1.95V	PWR_CL_DDR_52_195	1	R	0x00
[237]	Power class for 200MHz, at VCCQ =1.95V, VCC = 3.6V	PWR_CL_200_195	1	R	0x00
[236]	Power class for 200MHz, at VCCQ=1.3V, VCC = 3.6V	PWR_CL_200_130	1	R	0x00
[235]	Minimum Write Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_W_8_52	1	R	0x00
[234]	Minimum Read Performance for 8bit at 52MHz in DDR mode	MIN_PERF_DDR_R_8_52	1	R	0x00
[233]	Reserved	-	1	-	0x00
[232]	TRIM Multiplier	TRIM_MULT	1	R	0x11
[231]	Secure Feature support	SEC_FEATURE_SUPPORT	1	R	0x55
[230]	Secure Erase Multiplier	SEC_ERASE_MULT	1	R	0xF7
[229]	Secure TRIM Multiplier	SEC_TRIM_MULT	1	R	0xF7
[228]	Boot information	BOOT_INFO	1	R	0x07
[227]	Reserved	-	1	R	0x00
[226]	Boot partition size	BOOT_SIZE_MULT	1	R	0x40
[225]	Access size	ACC_SIZE	1	R	0x08
[224]	High-capacity erase unit size	HC_ERASE_GRP_SIZE	1	R	0x01
[223]	High-capacity erase timeout	ERASE_TIMEOUT_MULT	1	R	0x11
[222]	Reliable write sector count	REL_WR_SEC_C	1	R	0x01
[221]	High-capacity write protect group size	HC_WP_GRP_SIZE	1	R	0x10
[220]	Sleep current (V <sub>CC</sub> )	S_C_VCC	1	R	0x08
[219]	Sleep current (V <sub>CCQ</sub> )	S_C_VCCQ	1	R	0x08
[218]	Production state awareness timeout	PRODUCTION_STATE_AWARENESS_TIMEOUT	1	R	0x14
[217]	Sleep/awake timeout	S_A_TIMEOUT	1	R	0x15
[216]	Sleep Notification Timeout	SLEEP_NOTIFICATION_TIME	1	R	0x10
[215:212]	Sector Count	SEC_COUNT	4	R	0x01CF8000
[211]	Sector Write Protection Information	SECURE_WP_INFO	1	R	0x01
[210]	Minimum Write Performance for 8bit at 52MHz	MIN_PERF_W_8_52	1	R	0x08
[209]	Minimum Read Performance 8bit at 52MHz	MIN_PERF_R_8_52	1	R	0x08
[208]	Minimum Write Performance for 8bit at 26MHz, for 4bit at 52MHz	MIN_PERF_W_8_26_4_52	1	R	0x08
[207]	Minimum Read Performance for 8 bit at 26MHz, for 4bit at 52MHz	MIN_PERF_R_8_26_4_52	1	R	0x08
[206]	Minimum Write Performance for 4bit at 26MHz	MIN_PERF_W_4_26	1	R	0x08
[205]	Minimum Read Performance for 4bit at 26MHz	MIN_PERF_R_4_26	1	R	0x08



CSD-slice	Name	Field	Size (Bytes)	Cell Type	Value
[204]	Reserved	-	1	-	0x00
[203]	Power class for 26MHz at 3.6V	PWR_CL_26_360	1	R	0x00
[202]	Power class for 52MHz at 3.6V	PWR_CL_52_360	1	R	0x00
[201]	Power class for 26MHz at 1.95V	PWR_CL_26_195	1	R	0x00
[200]	Power class for 52MHz at 1.95V	PWR_CL_52_195	1	R	0x00
[199]	Partition switching timing	PARTITION_SWITCH_TIME	1	R	0xFF
[198]	Out-of-interrupt busy timing	OUT_OF_INTERRUPT_TIME	1	R	0xFF
[197]	I/O Driver Strength	DRIVER_STRENGTH	1	R	0x1F
[196]	Device Type	DEVICE_TYPE	1	R	0x57
[195]	Reserved	-	1	-	0x00
[194]	CSD structure version	CSD_STRUCTURE	1	R	0x02
[193]	Reserved	-	1	-	0x00
[192]	Extended CSD revision	EXT_CSD_REV	1	R	0x08
[191]	Command Set	CMD_SET	1	R/W/E_P	0x00
[190]	Reserved	-	1	-	0x00
[189]	Command set revision	CMD_SET_REV	1	R	0x00
[188]	Reserved	-	1	-	0x00
[187]	Power class <sup>Note 1</sup>	POWER_CLASS	1	R/W/E_P	0x00
[186]	Reserved	-	1	-	0x00
[185]	High-speed interface timing	HS_TIMING	1	R/W/E_P	0x01
[184]	Strobe Support	STROBE_SUPPORT	1	R	0x01
[183]	Bus width mode	BUS_WIDTH	1	W/E_P	0x02
[182]	Reserved	-	1	-	0x00
[181]	Erased memory content	ERASED_MEM_CONT	1	R	0x00
[180]	Reserved	-	1	-	0x00
[179]	Partition configuration	PARTITION_CONFIG	1	R/W/E & R/W/E_P	0x00
[178]	Boot config protection	BOOT_CONFIG_PROT	1	R/W & R/W/C_P	0x00
[177]	Boot bus Conditions	BOOT_BUS_CONDITIONS	1	R/W/E	0x00
[176]	Reserved	-	1	-	0x00
[175]	High-density erase group definition	ERASE_GROUP_DEF	1	R/W/E_P	0x00
[174]	Boot write protection status registers	BOOT_WP_STATUS	1	R	0x00
[173]	Boot area write protection register	BOOT_WP	1	R/W & R/W/C_P	0x00
[172]	Reserved	-	1	-	0x00
[171]	User area write protection register	USER_WP	1	R/W, R/W/C_P & R/W/E_P	0x00
[170]	Reserved	-	1	-	0x00
[169]	FW configuration	FW_CONFIG	1	R/W	0x00

CSD-slice	Name	Field	Size (Bytes)	Cell Type	Value
[168]	RPMB Size	RPMB_SIZE_MULT	1	R	0x20
[167]	Write reliability setting register	WR_REL_SET	1	R/W	0x00
[166]	Write reliability parameter register	WR_REL_PARAM	1	R	0x15
[165]	Start Sanitize operation	SANITIZE_START	1	W/E_P	0x00
[164]	Manually start background operations	BKOPS_START	1	W/E_P	0x00
[163]	Enable background operations handshake	BKOPS_EN	1	R/W & R/W/E	0x00
[162]	H/W reset function	RST_n_FUNCTION	1	R/W	0x00
[161]	HPI management	HPI_MGMT	1	R/W/E_P	0x00
[160]	Partitioning Support	PARTITIONING_SUPPORT	1	R	0x07
[159:157]	Max Enhanced Area Size <sup>Note 2</sup>	MAX_ENH_SIZE_MULT	3	R	0x00003D
[156]	Partitions attribute	PARTITIONS_ATTRIBUTE	1	R/W	0x00
[155]	Partitioning Setting	PARTITION_SETTING_COMPLETED	1	R/W	0x00
[154:143]	General Purpose Partition Size <sup>Note 3</sup>	GP_SIZE_MULT	12	R/W	0x00
[142:140]	Enhanced User Data Area Size <sup>Note 4</sup>	ENH_SIZE_MULT	3	R/W	0x00
[139:136]	Enhanced User Data Start Address	ENH_START_ADDR	4	R/W	0x00
[135]	Reserved	-	1	-	0x00
[134]	Bad Block Management mode	SEC_BAD_BLK_MGMNT	1	R/W	0x00
[133]	Production state awareness <sup>Note 6</sup>	PRODUCTION_STATE_AWARENESS	1	R/W/E	0x00
[132]	Package Case Temperature is controlled <sup>Note 1</sup>	TCASE_SUPPORT	1	W/E_P	0x00
[131]	Periodic Wake-up <sup>Note 1</sup>	PERIODIC_WAKEUP	1	R/W/E	0x00
[130]	Program CID/CSD in DDR mode support	PROGRAM_CID_CSD_DDR_SUPPORT	1	R	0x01
[129:128]	Reserved	-	2	-	All '0'
[127:64]	Vendor Specific Fields	VENDOR_SPECIFIC_FIELD	64	-	-
[63]	Native sector size	NATIVE_SECTOR_SIZE	1	R	0x00
[62]	Sector size emulation	USE_NATIVE_SECTOR	1	R/W	0x00
[61]	Sector size	DATA_SECTOR_SIZE	1	R	0x00
[60]	1st initialization after disabling sector size emulation	INI_TIMEOUT_EMU	1	R	0x00
[59]	Class 6 commands control	CLASS_6_CTRL	1	R/W/E_P	0x00
[58]	Number of addressed group to be Released	DYNCAP_NEEDED	1	R	0x00
[57:56]	Exception events control	EXCEPTION_EVENTS_CTRL	2	R/W/E_P	0x00
[55:54]	Exception events status	EXCEPTION_EVENTS_STATUS	2	R	All '0'
[53:52]	Extended partitions attribute <sup>Note 1</sup>	EXT_PARTITIONS_ATTRIBUTE	2	R/W	0x00
[51:37]	Context configuration	CONTEXT_CONF	15	R/W/E_P	0x00
[36]	Packed command status	PACKED_COMMAND_STATUS	1	R	0x00
[35]	Packed command failure index	PACKED_FAILURE_INDEX	1	R	0x00
[34]	Power Off Notification <sup>Note 5</sup>	POWER_OFF_NOTIFICATION	1	R/W/E_P	0x00
[33]	Control to turn the Cache ON/OFF	CACHE_CTRL	1	R/W/E_P	0x00

CSD-slice	Name	Field	Size (Bytes)	Cell Type	Value
[32]	Flushing of the cache	FLUSH_CACHE	1	W/E_P	0x00
[31]	Control to turn the Barrier ON/OFF	BARRIER_CTRL	1	R/W	0x00
[30]	Mode config	MODE_CONFIG	1	R/W/E_P	0x00
[29]	Mode operation codes	MODE_OPERATION_CODES	1	W/E_P	0x00
[28:27]	Reserved	-	2	-	All '0'
[26]	FFU status	FFU_STATUS	1	R	0x00
[25:22]	Pre loading data size <sup>Note 6</sup>	PRE_LOADING_DATA_SIZE	4	R/W/E_P	0x00
[21:18]	Max pre loading data size	MAX_PRE_LOADING_DATA_SIZE	4	R	0x00994000
[17]	Product state awareness enablement <sup>Note 6</sup>	PRODUCT_STATE_AWARENESS_ENABLEMENT	1	R/W/E & R	0x01
[16]	Secure Removal Type	SECURE_REMOVAL_TYPE	1	R/W & R	0x01
[15]	Command Queue Mode Enable	CMDQ_MODE_EN	1	R/W/E_P	0x00
[14:0]	Reserved	-	15	-	All '0'

Note 1: Although these fields can be re-written by host, TOSHIBA Memory e-MMC does not support.

Note 2: Max Enhanced Area Size (MAX\_ENH\_SIZE\_MULT [159:157]) has to be calculated by following formula.

Max Enhanced Area = MAX\_ENH\_SIZE\_MULT x HC\_WP\_GRP\_SIZE x HC\_ERASE\_GRP\_SIZE x 512kBytes

$$\sum_{i=1}^4 \text{Enhanced general partition size}(i) + \text{Enhanced user data area} \leq \text{Max enhanced area}$$

Note 3: General Purpose Partition Size (GP\_SIZE\_MULT\_GP0 - GP\_SIZE\_MULT\_GP3 [154:143]) has to be calculated by following formula.

$$\begin{aligned} \text{General\_Purpose\_Partition\_X Size} = & (\text{GP\_SIZE\_MULT\_X\_2} \times 2^{16} + \text{GP\_SIZE\_MULT\_X\_1} \times 2^8 \\ & + \text{GP\_SIZE\_MULT\_X\_0} \times 2^0) \times \text{HC\_WP\_GRP\_SIZE} \\ & \times \text{HC\_ERASE\_GRP\_SIZE} \times 512\text{kBytes} \end{aligned}$$

Note 4: Enhanced User Data Area Size (ENH\_SIZE\_MULT [142:140]) has to be calculated by following formula.

$$\begin{aligned} \text{Enhanced User Data Area x Size} = & (\text{ENH\_SIZE\_MULT\_2} \times 2^{16} + \text{ENH\_SIZE\_MULT\_1} \times 2^8 \\ & + \text{ENH\_SIZE\_MULT\_0} \times 2^0) \times \text{HC\_WP\_GRP\_SIZE} \\ & \times \text{HC\_ERASE\_GRP\_SIZE} \times 512\text{kBytes} \end{aligned}$$

Note 5: Toshiba Memory recommends to issue the Power Off Notification before turning off the device, especially when cache is on or AUTO\_EN(BKOPS\_EN[163]:bit1) is set to '1b'.

Note 6: - Pre loading data size = PRE\_LOADING\_DATA\_SIZE x Sector Size

Pre-loading data size should be multiple of 4KB and the pre-loading data should be written by multiple of 4KB chunk size, aligned with 4KB address. This is because the valid data size will be treated as 4KB when host writes data less than 4KB.

- If the host continues to write data in Normal state (after it wrote PRE\_LOADING\_DATA\_SIZE amount of data) and before soldering, the pre-loading data might be corrupted after soldering.
- If a power cycle is occurred during the data transfer, the amount of data written to device is not clear. Therefore in this case, host should erase the entire pre-loaded data and set again PRE\_LOADING\_DATA\_SIZE[25:22], PRODUCTION\_STATE\_AWARENESS[133], and PRODUCT\_STATE\_AWARENESS\_ENABLEMENT[17].

## ELECTRICAL CHARACTERISTICS

### DC Characteristics

#### Absolute Maximum Ratings

The absolute maximum ratings of a semiconductor device are a set of specified parameter values, which must not be exceeded during operation, even for an instant.

If any of these rating would be exceeded during operation, the device electrical characteristics may be irreparably altered and the reliability and lifetime of the device can no longer be guaranteed. Moreover, these operations with exceeded ratings may cause break down, damage, and/or degradation to any other equipment. Applications using the device should be designed such that each maximum rating will never be exceeded in any operating conditions.

Before using, creating, and/or producing designs, refer to and comply with the precautions and conditions set forth in this document.

Parameter	Symbol	Test Conditions	Min	Max	Unit
Supply voltage 1	$V_{CC}$	-	-0.5	4.7	V
Supply voltage 2	$V_{CCQ}$	-	-0.5	1.98	V
Voltage Input	$V_{IO}$	-	-0.5	1.98	V

### General

Parameter	Symbol	Test Conditions	Min	Max	Unit
Peak voltage on all lines	-	-	-0.5	$V_{CCQ}+0.5$	V
All Inputs					
Input Leakage Current (before initialization sequence <sup>Note 1</sup> and/or the internal pull up resistors connected)	-	-	-100	100	$\mu$ A
Input Leakage Current (after initialization sequence and the internal pull up resistors disconnected)	-	-	-2	2	$\mu$ A
All Outputs					
Output Leakage Current (before initialization sequence)	-	-	-100	100	$\mu$ A
Output Leakage Current (after initialization sequence)	-	-	-2	2	$\mu$ A

Note 1: Initialization sequence is defined in Power-Up chapter of JEDEC/MMCA Standard

### Power Supply Voltage

Parameter	Symbol	Test Conditions	Min	Max	Unit
Supply voltage 1	$V_{CC}$	-	2.7	3.6	V
Supply voltage 2	$V_{CCQ}$	-	1.7	1.95	V
			2.7	3.6	V

Note 1: Once the power supply  $V_{CC}$  or  $V_{CCQ}$  falls below the minimum guaranteed voltage (for example, upon sudden power fail), the voltage level of  $V_{CC}$  or  $V_{CCQ}$  shall be kept less than 0.5 V for at least 1ms before it goes beyond 0.5 V again.

Note 2: The host and device I/O power ( $V_{CCQ}$ ) shall be provided from same power supply.

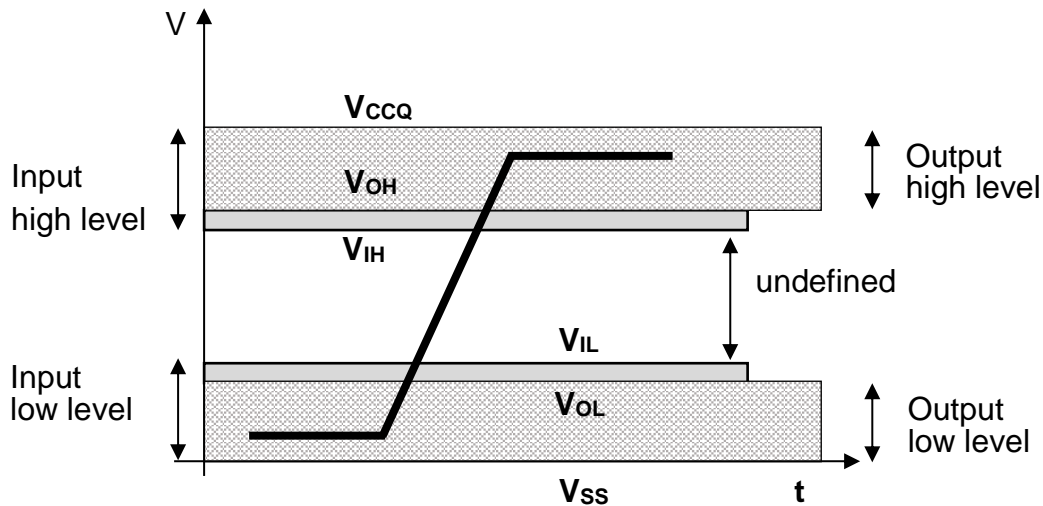
**Supply Current**

Parameter		Symbol	Interleave Operation	Mode	V <sub>CCQ</sub>	Min		Max		Unit
						I <sub>CCQ</sub>	I <sub>CC</sub>	I <sub>CCQ</sub>	I <sub>CC</sub>	
Operation (RMS)	Read	I <sub>ROP</sub>	Non Interleave	SDR	1.8V	—	—	TBD	TBD	mA
				DDR	1.8V	—	—	TBD	TBD	mA
				HS200	1.8V	—	—	TBD	TBD	mA
				HS400	1.8V	—	—	TBD	TBD	mA
	Write	I <sub>WOP</sub>	Non Interleave	SDR	1.8V	—	—	TBD	TBD	mA
				DDR	1.8V	—	—	TBD	TBD	mA
				HS200	1.8V	—	—	TBD	TBD	mA
				HS400	1.8V	—	—	TBD	TBD	mA

**Internal resistance and Device capacitance**

Parameter	Symbol	Test Conditions	Min	Max	Unit
Single device capacitance	C <sub>DEVICE</sub>	—	—	6	pF
Internal pull up resistance DAT1 – DAT7	R <sub>INT</sub>	—	10	150	kΩ

**Bus Signal Levels**



**Open-Drain Mode Bus Signal Level**

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	VOH	V <sub>CCQ</sub> - 0.2	—	V	Note 1
Output LOW voltage	VOL	—	0.3	V	I <sub>OL</sub> = 2 mA

Note 1: Because VOH depends on external resistance value (including outside the package), this value does not apply as device specification. Host is responsible to choose the external pull-up and open drain resistance value to meet VOH Min value.

**Push-Pull Mode Bus Signal Level (High-Voltage)**

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	VOH	0.75 * V <sub>CCQ</sub>	—	V	IOH = -100 μA @ V <sub>CCQ</sub> min
Output LOW voltage	VOL	—	0.125 * V <sub>CCQ</sub>	V	IOL = 100 μA @ V <sub>CCQ</sub> min
Input HIGH voltage	VIH	0.625 * V <sub>CCQ</sub>	V <sub>CCQ</sub> + 0.3	V	
Input LOW voltage	VIL	V <sub>SS</sub> - 0.3	0.25 * V <sub>CCQ</sub>	V	

**Push-Pull Mode Bus Signal Level (Dual-Voltage)**

Parameter	Symbol	Min	Max	Unit	Conditions
Output HIGH voltage	VOH	V <sub>CCQ</sub> - 0.45	—	V	IOH = -2mA
Output LOW voltage	VOL	—	0.45	V	IOL = 2mA
Input HIGH voltage	VIH	0.65 * V <sub>CCQ</sub>	V <sub>CCQ</sub> + 0.3	V	
Input LOW voltage	VIL	V <sub>SS</sub> - 0.3	0.35 * V <sub>CCQ</sub>	V	

### Driver Types Definition

In JEDEC, Driver Type-0 is defined as mandatory for e-MMC HS200&HS400 Device. While four additional Driver Types (1, 2, 3 and 4) are defined as optional, to allow the support of wider Host loads. The Host may select the most appropriate Driver Type of the Device (if supported) to achieve optimal signal integrity performance.

Driver Type-0 is targeted for transmission line, based distributed system with 50Ω nominal line impedance. Therefore, it is defined as 50Ω nominal driver. The nominal line impedance should be kept as 50Ω even if Driver Type would be changed.

For HS200, when tested with  $C_L = 15\text{pF}$  Driver Type-0 shall meet all AC characteristics and HS200 Device output timing requirements. The test circuit defined in section 10.5.4.3 of JEDEC/MMCA Standard 5.1 is used for testing of Driver Type-0.

For HS400, when tested with the reference load defined in page 27 HS400 reference load figure, Driver Type-0 or Driver Type-1 or Driver Type-4 shall meet all AC characteristics and HS400 Device output timing requirements.

Driver Type	TOSHIBA e-MMC	Nominal Impedance (Driver strength)	Approximated driving capability compared to Type-0	Remark
0	Supported	50 Ω (18mA)	x1	Default Driver Type
1	Supported	33 Ω (27mA)	x1.5	Recommendation at HS400 under the condition of JEDEC standard reference load.
2	Supported	66 Ω (14mA)	x0.75	
3	Supported	100 Ω (9mA)	x0.5	
4	Supported	40 Ω (23mA)	x1.2	Recommendation at HS400 under the condition of JEDEC standard reference load.

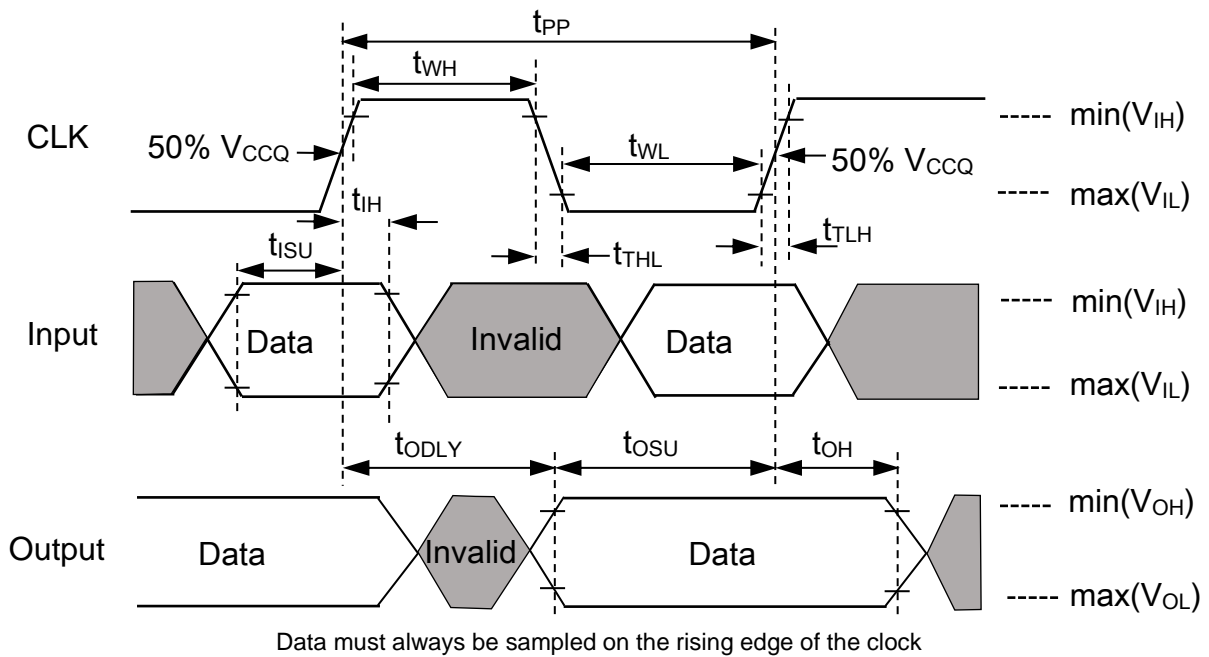
Note: Nominal impedance is defined by I-V characteristics of output driver at 0.9V when  $V_{CCQ} = 1.8\text{V}$ .

**\*The most suitable setting for user's operating environment should be selected.**

**At HS400, Toshiba Memory recommends Driver Type-1 and Type-4. This is because they meet all AC characteristics and Device output timing requirements under the condition of JEDEC standard reference load.**



**Bus Timing**



**Device Interface Timings (High-speed interface timing)**

Parameter	Symbol	Min	Max	Unit	Remark
Clock CLK <sup>Note 1</sup>					
Clock frequency Data Transfer Mode (PP) <sup>Note 2</sup>	$f_{pp}$	0	52 <sup>Note 3</sup>	MHz	$C_L \leq 30\text{pF}$ Tolerance: +100kHz
Clock frequency Identification Mode (OD)	$f_{OD}$	0	400	kHz	Tolerance: +20kHz
Clock high time	$t_{WH}$	6.5	—	ns	$C_L \leq 30\text{pF}$
Clock low time	$t_{WL}$	6.5	—	ns	$C_L \leq 30\text{pF}$
Clock rise time <sup>Note 4</sup>	$t_{TLH}$	—	3	ns	$C_L \leq 30\text{pF}$
Clock fall time	$t_{THL}$	—	3	ns	$C_L \leq 30\text{pF}$
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	$t_{ISU}$	3	—	ns	$C_L \leq 30\text{pF}$
Input hold time	$t_{IH}$	3	—	ns	$C_L \leq 30\text{pF}$
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer	$t_{ODLY}$	—	13.7	ns	$C_L \leq 30\text{pF}$
Output hold time	$t_{OH}$	2.5	—	ns	$C_L \leq 30\text{pF}$
Signal rise time <sup>Note 5</sup>	$t_{rise}$	—	3	ns	$C_L \leq 30\text{pF}$
Signal fall time	$t_{fall}$	—	3	ns	$C_L \leq 30\text{pF}$

Note 1: CLK timing is measured at 50% of  $V_{CCQ}$ .

Note 2: This product shall support the full frequency range from 0 MHz - 26 MHz, or 0 MHz - 52 MHz.

Note 3: Device can operate as high-speed interface timing at 26MHz clock frequency.

Note 4: CLK rise and fall times are measured by  $\min(V_{IH})$  and  $\max(V_{IL})$ .

Note 5: Inputs CMD, DAT rise and fall times are measured by  $\min(V_{IH})$  and  $\max(V_{IL})$ , and outputs CMD, DAT rise and fall times are measured by  $\min(V_{OH})$  and  $\max(V_{OL})$ .

**Device Interface Timings (Backward-compatible interface timing)**

Parameter	Symbol	Min	Max	Unit	Remark <sup>Note 1</sup>
Clock CLK <sup>Note 2</sup>					
Clock frequency Data Transfer Mode (PP) <sup>Note 3</sup>	f <sub>pp</sub>	0	26	MHz	C <sub>L</sub> ≤ 30pF
Clock frequency Identification Mode (OD)	f <sub>OD</sub>	0	400	kHz	
Clock high time	t <sub>WH</sub>	10	—	ns	C <sub>L</sub> ≤ 30pF
Clock low time	t <sub>WL</sub>	10	—	ns	C <sub>L</sub> ≤ 30pF
Clock rise time <sup>Note 4</sup>	t <sub>TLH</sub>	—	10	ns	C <sub>L</sub> ≤ 30pF
Clock fall time	t <sub>THL</sub>	—	10	ns	C <sub>L</sub> ≤ 30pF
Inputs CMD,DAT (referenced to CLK)					
Input set-up time	t <sub>ISU</sub>	3	—	ns	C <sub>L</sub> ≤ 30pF
Input hold time	t <sub>IH</sub>	3	—	ns	C <sub>L</sub> ≤ 30pF
Outputs CMD,DAT (referenced to CLK)					
Output set-up time <sup>Note 5</sup>	t <sub>OSU</sub>	11.7	—	ns	C <sub>L</sub> ≤ 30pF
Output hold time <sup>Note 5</sup>	t <sub>OH</sub>	8.3	—	ns	C <sub>L</sub> ≤ 30pF

Note 1: The e-MMC must always start with the backward-compatible interface timing. The timing mode can be switched to high-speed interface timing by the host sending the SWITCH command (CMD6) with the argument for high-speed interface select.

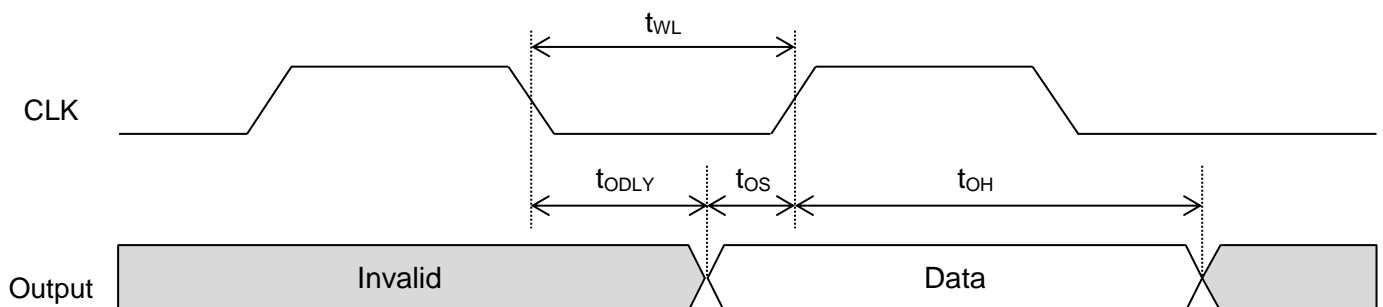
Note 2: CLK timing is measured at 50% of V<sub>CCQ</sub>.

Note 3: For compatibility with e-MMCs that support the v4.2 standard or earlier, host should not use >26MHz before switching to high-speed interface timing.

Note 4: CLK rise and fall times are measured by min (V<sub>IH</sub>) and max (V<sub>IL</sub>).

Note 5: t<sub>OSU</sub> and t<sub>OH</sub> are defined as values from clock rising edge. However, the e-MMC device will utilize clock falling edge to output data in backward compatibility mode. Therefore, it is recommended for hosts either to set t<sub>WL</sub> value as long as possible within the range which will not go over t<sub>CK</sub> - t<sub>OH</sub>(min) in the system or to use slow clock frequency, so that host could have data set up margin for the device.

Toshiba e-MMC device utilize clock falling edge to output data in backward compatibility mode.  
Host should optimize the timing in order to have data set up margin as follows.

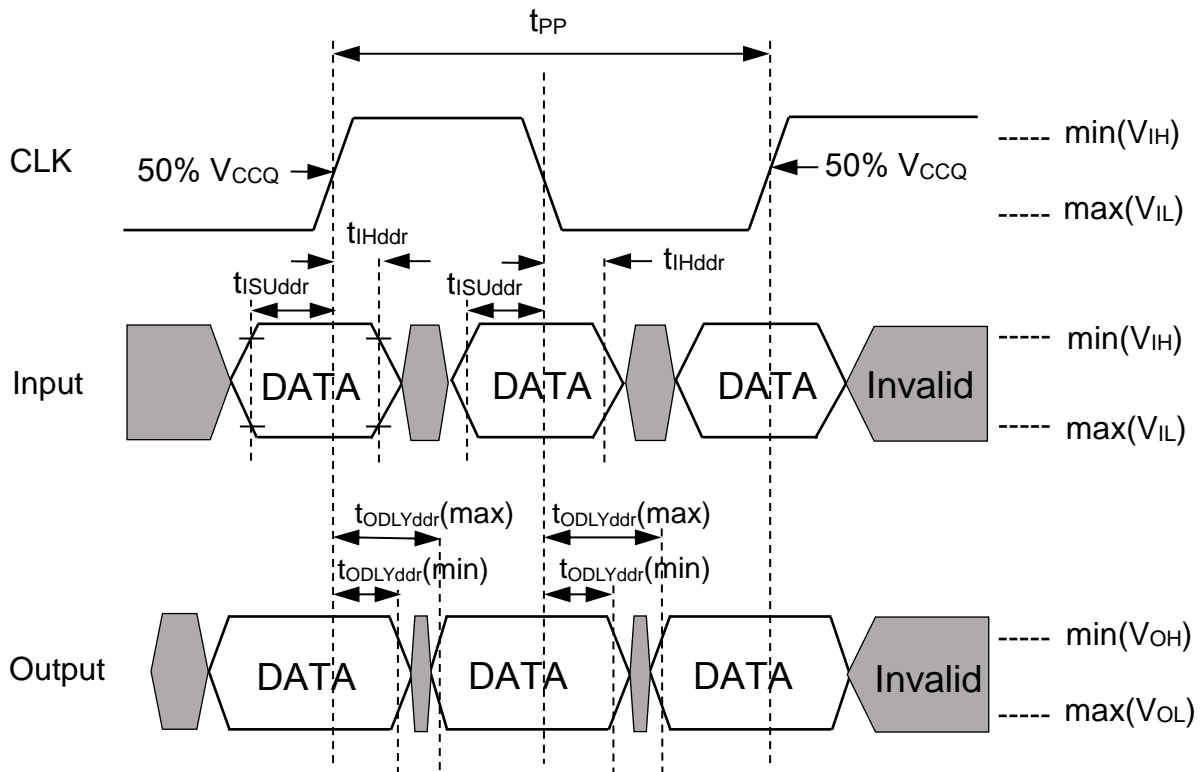


$$t_{OSU} (\text{min}) = t_{WL}(\text{min}) - t_{ODLY}(\text{max } 8\text{ns})$$

**Figure 2 Output timing**

**Bus Timing for DAT signals for during 2x data rate operation**

These timings applies to the DAT[7:0] signals only when the device is configured for dual data mode operation. In this dual data mode, the DAT signals operates synchronously of both the rising and the falling edges of CLK. The CMD signal still operates synchronously of the rising edge of CLK and therefore complies with the bus timing specified in High-speed interface timing or Backward-compatible interface timing.



In DDR mode data on DAT[7:0] lines are sampled on both edges of the clock (not applicable for CMD line).

**High-speed dual data rate interface timings**

Parameter	Symbol	Min	Max	Unit	Remark
Input CLK <sup>Note 1</sup>					
Clock duty cycle		45	55	%	Includes jitter, phase noise
Clock rise time	$t_{TLH}$	—	3	ns	$C_L \leq 30\text{pF}$
Clock fall time	$t_{THL}$	—	3	ns	$C_L \leq 30\text{pF}$
Input CMD (referenced to CLK-SDR mode)					
Input set-up time	$t_{ISUddr}$	3	—	ns	$C_L \leq 20\text{pF}$
Input hold time	$t_{IHddr}$	3	—	ns	$C_L \leq 20\text{pF}$
Output CMD (referenced to CLK-SDR mode)					
Output delay time during data transfer	$t_{ODLY}$	—	13.7	ns	$C_L \leq 20\text{pF}$
Output hold time	$t_{OH}$	2.5	—	ns	$C_L \leq 20\text{pF}$
Signal rise time	$t_{RISE}$	—	3	ns	$C_L \leq 20\text{pF}$
Signal fall time	$t_{FALL}$	—	3	ns	$C_L \leq 20\text{pF}$

Parameter	Symbol	Min	Max	Unit	Remark
Input DAT (referenced to CLK-DDR mode)					
Input set-up time	$t_{ISUddr}$	2.5	—	ns	$C_L \leq 20pF$
Input hold time	$t_{IHddr}$	2.5	—	ns	$C_L \leq 20pF$
Output DAT (referenced to CLK-DDR mode)					
Output delay time during data transfer	$t_{ODLYddr}$	1.5	7	ns	$C_L \leq 20pF$
Signal rise time (all signals) <sup>Note 2</sup>	$t_{RISE}$	—	2	ns	$C_L \leq 20pF$
Signal fall time (all signals)	$t_{FALL}$	—	2	ns	$C_L \leq 20pF$

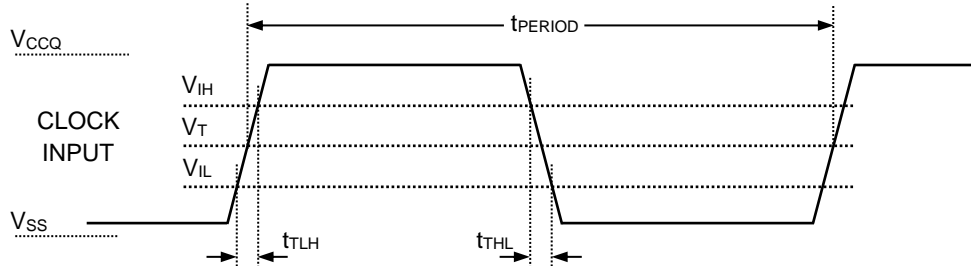
Note 1: CLK timing is measured at 50% of  $V_{CCQ}$ .

Note 2: Inputs DAT rise and fall times are measured by min ( $V_{IH}$ ) and max ( $V_{IL}$ ), and outputs DAT rise and fall times are measured by min ( $V_{OH}$ ) and max ( $V_{OL}$ ).

**Bus Timing Specification in HS200 mode**

**HS200 Clock Timing**

Host CLK Timing in HS200 mode shall conform to the timing specified in following figure and Table. CLK input shall satisfy the clock timing over all possible operation and environment conditions. CLK input parameters should be measured while CMD and DAT lines are stable high or low, as close as possible to the Device. The maximum frequency of HS200 is 200MHz. Hosts can use any frequency up to the maximum that HS200 mode allows.

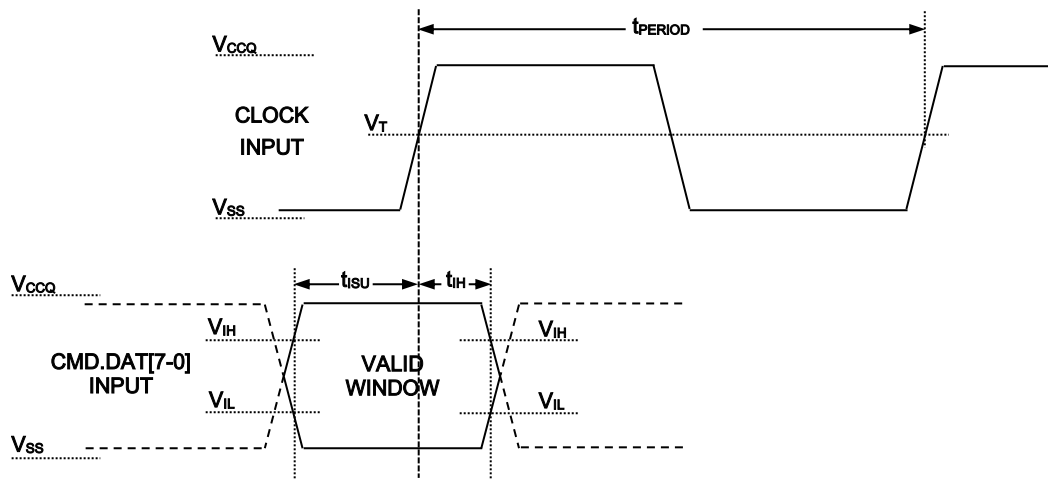


Note 1:  $V_{IH}$  denote  $V_{IH(min)}$  and  $V_{IL}$  denotes  $V_{IL(max)}$ .

Note 2:  $V_T = 50\%$  of  $V_{CCQ}$ , indicates clock reference point for timing measurements.

Symbol	Min	Max	Unit	Remark
$t_{PERIOD}$	5	—	ns	200MHz (max.), between rising edges
$t_{TLH}, t_{THL}$	—	$0.2 * t_{PERIOD}$	ns	$t_{TLH}, t_{THL} < 1\text{ns}$ (max.) at 200MHz, $C_{DEVICE}=6\text{pF}$ , The absolute maximum value of $t_{TLH}, t_{THL}$ is 10ns regardless of clock frequency.
Duty Cycle	30	70	%	

**HS200 Device Input Timing**



Note 1:  $t_{ISU}$  and  $t_{IH}$  are measured at  $V_{IL(max)}$  and  $V_{IH(min)}$ .

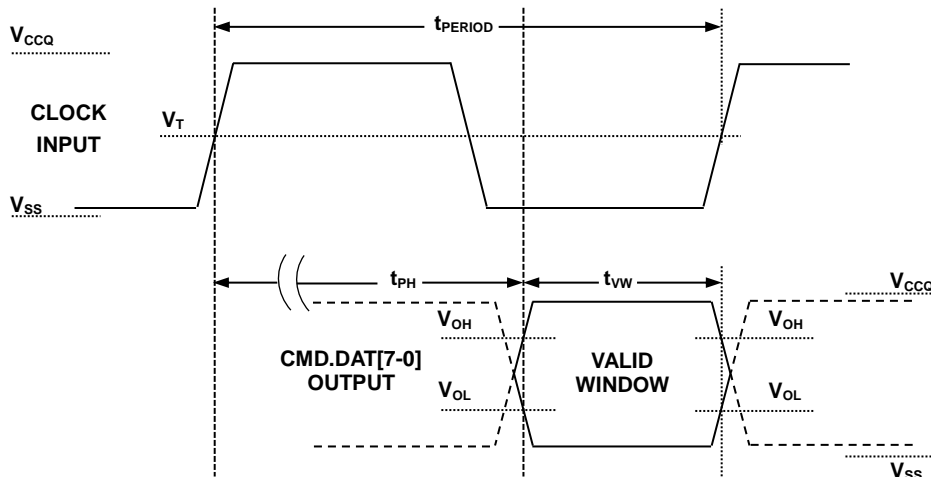
Note 2:  $V_{IH}$  denote  $V_{IH(min)}$  and  $V_{IL}$  denotes  $V_{IL(max)}$ .

Symbol	Min	Max	Unit	Remark
$t_{ISU}$	1.40	—	ns	$C_{DEVICE} \leq 6\text{pF}$
$t_{IH}$	0.8	—	ns	$C_{DEVICE} \leq 6\text{pF}$

**HS200 Device Output Timing**

$t_{PH}$  parameter is defined to allow device output delay to be longer than  $t_{PERIOD}$ . After initialization, the  $t_{PH}$  may have random phase relation to the clock. The Host is responsible to find the optimal sampling point for the Device outputs, while switching to the HS200 mode.

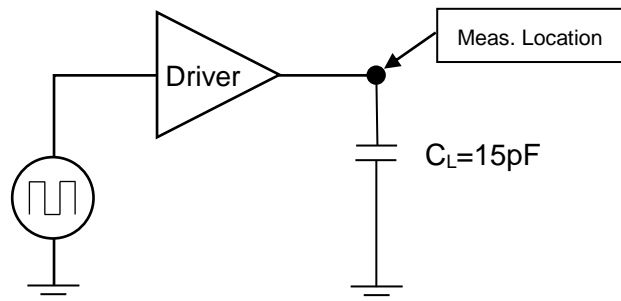
While setting the sampling point of data, a long term drift, which mainly depends on temperature drift, should be considered. The temperature drift is expressed by  $\Delta T_{PH}$ . Output valid data window ( $t_{VW}$ ) is available regardless of the drift ( $\Delta T_{PH}$ ) but position of data window varies by the drift.



Note:  $V_{OH}$  denotes  $V_{OH}(min)$  and  $V_{OL}$  denotes  $V_{OL}(max)$ .

Symbol	Min	Max	Unit	Remark <sup>Note 1</sup>
$t_{PH}$	0	2	UI	Device output momentary phase from CLK input to CMD or DAT lines output. Does not include a long term temperature drift.
$\Delta T_{PH}$	-350 ( $\Delta T = -20\text{ }^\circ\text{C}$ )	+1550 ( $\Delta T = 90\text{ }^\circ\text{C}$ )	ps	Delay variation due to temperature change after tuning. Total allowable shift of output valid window ( $t_{VW}$ ) from last system Tuning procedure. $\Delta T_{PH}$ is 2600ps for $\Delta T$ from $-25\text{ }^\circ\text{C}$ to $125\text{ }^\circ\text{C}$ during operation.
$t_{VW}$	0.575	—	UI	$t_{VW} = 2.88\text{ns}$ at 200MHz Using test circuit in following figure including skew among CMD and DAT lines created by the Device. Host path may add Signal Integrity induced noise, skews, etc. Expected $t_{VW}$ at Host input is larger than 0.475UI.

Note 1: Unit Interval (UI) is one bit nominal time. For example, UI=5ns at 200 MHz.

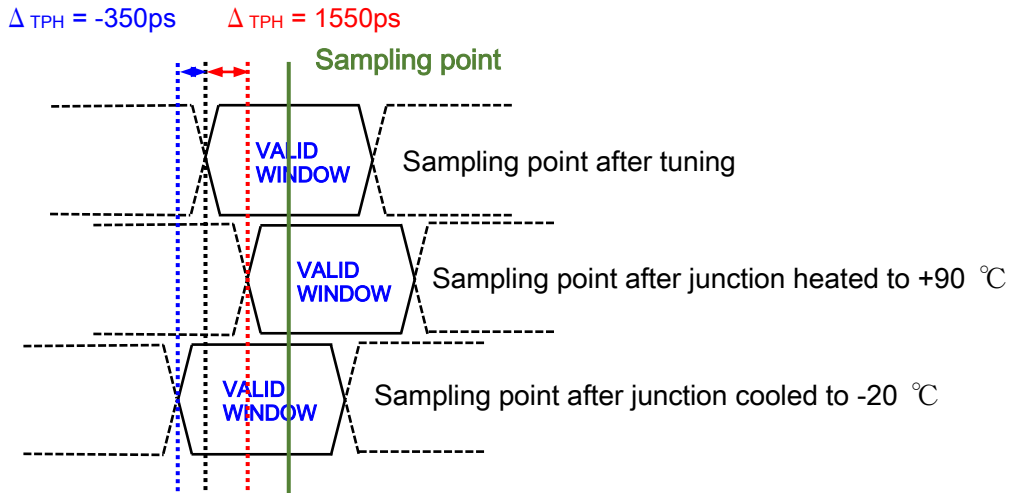


Note 1:  $C_L$  is total equivalent lumped capacitance for each Driver.

Note 2:  $C_L$  incorporates device die load, device package load and equivalent lumped load external to the device.

Note 3: In distributed transmission lines only part of the line capacitance considered as load for the Driver.

**$\Delta_{TPH}$  consideration**

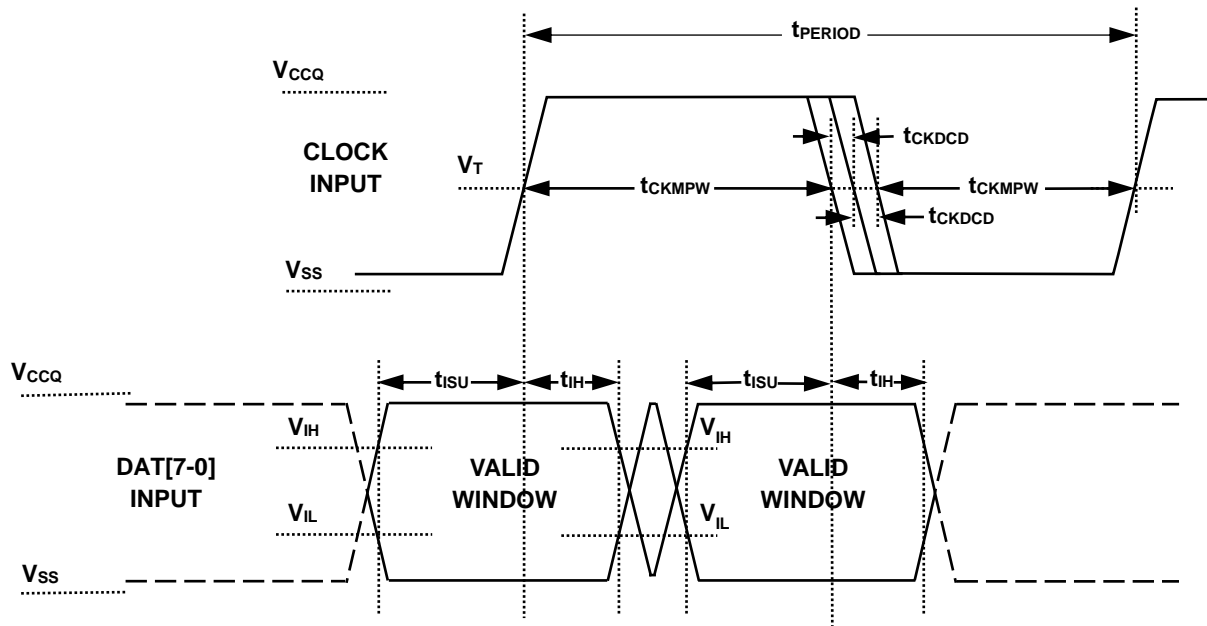


**Implementation Guide:**  
 Host should design to avoid sampling errors that may be caused by the  $\Delta_{TPH}$  drift.  
 It is recommended to perform tuning procedure while Device wakes up, after sleep.  
 One simple way to overcome the  $\Delta_{TPH}$  drift is by reduction of operating frequency.

**Bus Timing Specification in HS400 mode**

**HS400 Input Timing**

The CMD input timing for HS400 mode is the same as CMD input timing for HS200 mode.



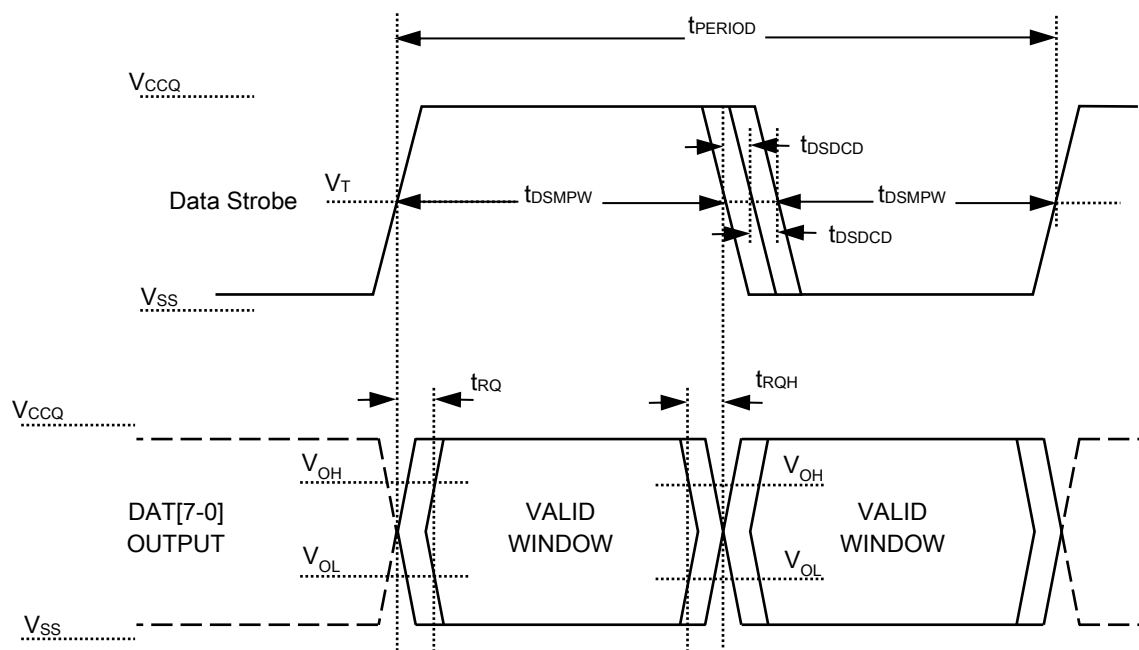
Note:  $V_T = 50\%$  of  $V_{CCQ}$ , indicates clock reference point for timing measurements.

Parameter	Symbol	Min	Max	Unit	Remark
Input CLK					
Cycle time data transfer mode	$t_{PERIOD}$	5	—	ns	200 MHz(max), between rising edges With respect to $V_T$
Slew rate	SR	1.125	—	V/ns	With respect to $V_{IH}/V_{IL}$
Duty cycle distortion	$t_{CKDCD}$	0.0	0.3	ns	Allowable deviation from an ideal 50% duty cycle. With respect to $V_T$ Includes jitter, phase noise
Minimum pulse width	$t_{CKMPW}$	2.2	—	ns	With respect to $V_T$
Input DAT (referenced to CLK)					
Input set-up time	$t_{ISUddr}$	0.4	—	ns	$C_{DEVICE} \leq 6$ pF With respect to $V_{IH}/V_{IL}$
Input hold time	$t_{IHddr}$	0.4	—	ns	$C_{DEVICE} \leq 6$ pF With respect to $V_{IH}/V_{IL}$
Slew rate	SR	1.125	—	V/ns	With respect to $V_{IH}/V_{IL}$



### HS400 Device Output Timing

The Data Strobe is used to read data in HS400 mode. The Data Strobe is toggled only during data read or CRC status response.

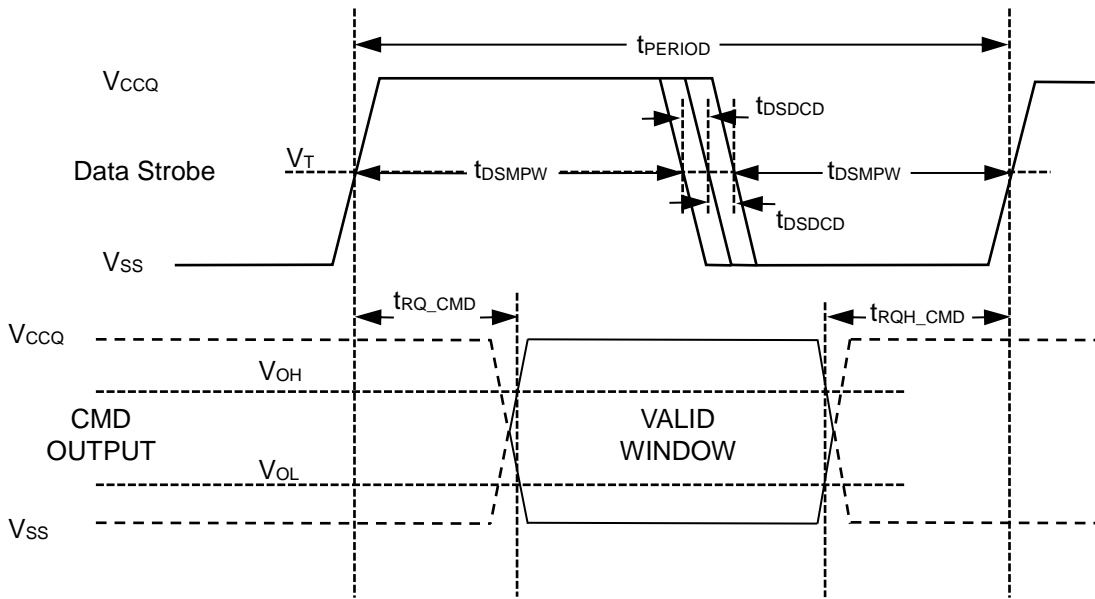


Note:  $V_T = 50\%$  of  $V_{CCQ}$ , indicates clock reference point for timing measurements.

Parameter	Symbol	Min	Max	Unit	Remark
Data Strobe					
Cycle time data transfer mode	$t_{PERIOD}$	5	—	ns	200 MHz(max), between rising edges With respect to $V_T$
Slew rate	SR	1.125	—	V/ns	With respect to $V_{OH}/V_{OL}$ and HS400 reference load
Duty cycle distortion	$t_{DSDCD}$	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion( $t_{CKDCD}$ ) With respect to $V_T$ Includes jitter, phase noise
Minimum pulse width	$t_{DSMPW}$	2.0	—	ns	With respect to $V_T$
Output DAT (referenced to Data Strobe)					
Output skew	$t_{RQ}$	—	0.4	ns	With respect to $V_{OH}/V_{OL}$ and HS400 reference load
Output hold skew	$t_{RQH}$	—	0.4	ns	With respect to $V_{OH}/V_{OL}$ and HS400 reference load
Slew rate	SR	1.125	—	V/ns	With respect to $V_{OH}/V_{OL}$ and HS400 reference load

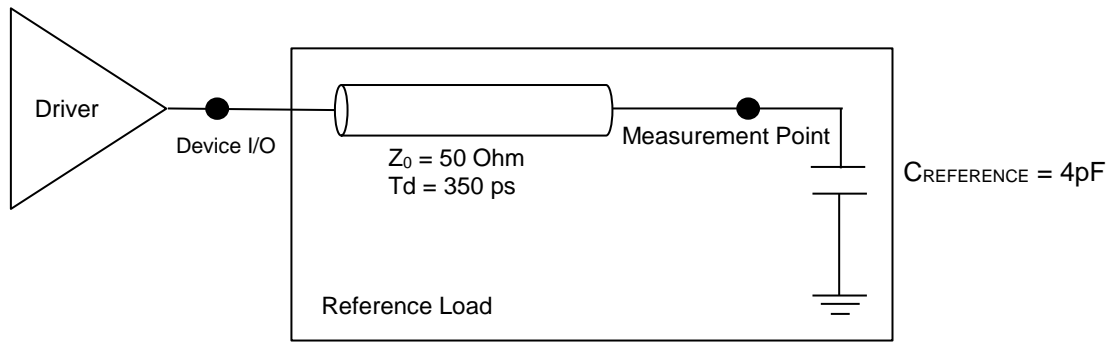
**HS400 Device Command Output Timing**

The Data Strobe is used to response of any command in HS400 mode.



Note:  $V_T = 50\%$  of  $V_{CCQ}$ , indicates clock reference point for timing measurements.

Parameter	Symbol	Min	Max	Unit	Remark
Data Strobe					
Cycle time data transfer mode	$t_{PERIOD}$	5	—	ns	200 MHz(max), between rising edges With respect to $V_T$
Slew rate	SR	1.125	—	V/ns	With respect to $V_{OH}/V_{OL}$ and HS400 reference load
Duty cycle distortion	$t_{DSDCD}$	0.0	0.2	ns	Allowable deviation from the input CLK duty cycle distortion( $t_{CKDCD}$ ) With respect to $V_T$ Includes jitter, phase noise
Minimum pulse width	$t_{DSMPW}$	2.0	—	ns	With respect to $V_T$
CMD Response (referenced to Data Strobe)					
Output skew (CMD)	$t_{RQ\_CMD}$	—	0.4	ns	With respect to $V_{OH}/V_{OL}$ and HS400 reference load
Output hold skew (CMD)	$t_{RQH\_CMD}$	—	0.4	ns	With respect to $V_{OH}/V_{OL}$ and HS400 reference load
Slew rate	SR	1.125	—	V/ns	With respect to $V_{OH}/V_{OL}$ and HS400 reference load



**Figure 3 HS400 reference load**

**HS400 Capacitance**

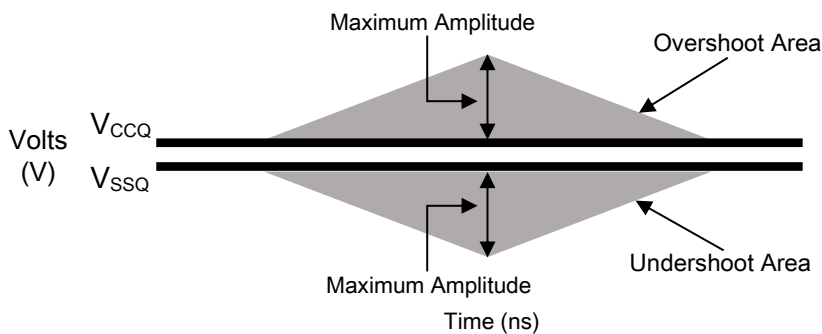
The Data Strobe is used to read data in HS400 mode. The Data Strobe is toggled only during data read or CRC status response.

Parameter	Symbol	Min	Typ.	Max	Unit	Remark
Pull-up resistance for CMD	R <sub>CMD</sub>	4.7		100 <sup>Note 1</sup>	kΩ	
Pull-up resistance for DAT0-7	R <sub>DAT</sub>	10		100 <sup>Note 1</sup>	kΩ	
Pull-down resistance for Data Strobe	R <sub>DS</sub>	10		100 <sup>Note 1</sup>	kΩ	
Internal pull up resistance DAT1-DAT7	R <sub>int</sub>	10		150	kΩ	
Single Device capacitance	C <sub>DEVICE</sub>			6	pF	

Note 1: Recommended maximum value is 50 kΩ for 1.8 V interface supply voltages.

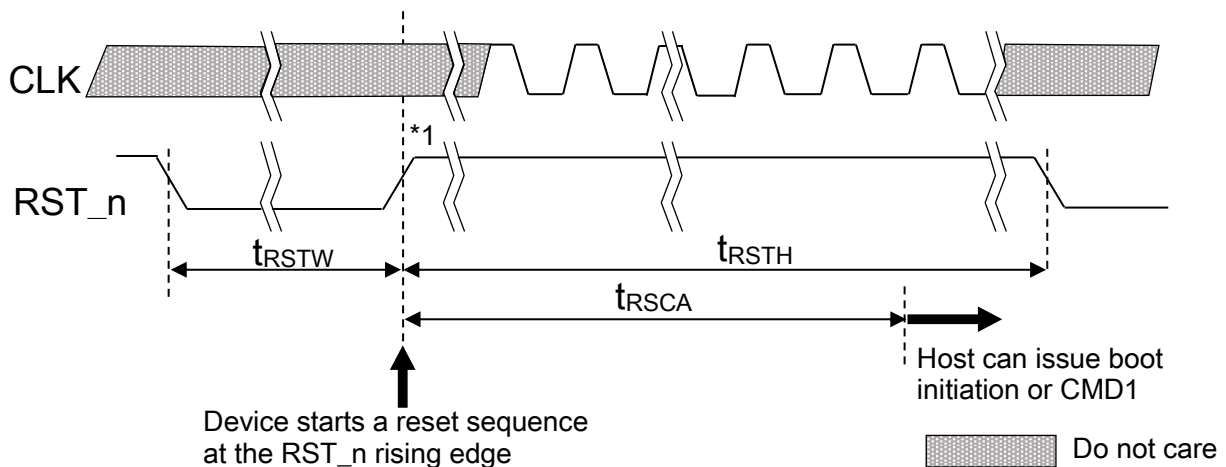
**Overshoot/Undershoot Specification**

		V <sub>CCQ</sub>	Unit
		1.70V - 1.95V	
Maximum peak amplitude allowed for overshoot area. (See Figure Overshoot/Undershoot definition)	Max	0.9	V
Maximum peak amplitude allowed for undershoot area. (See Figure Overshoot/Undershoot definition)	Max	0.9	V
Maximum area above V <sub>CCQ</sub> (See Figure Overshoot/Undershoot definition)	Max	1.5	V-ns
Maximum area below V <sub>SSQ</sub> (See Figure Overshoot/Undershoot definition)	Max	1.5	V-ns



**Figure 4 Overshoot/Undershoot definition**

**H/W Reset Operation**



\*1: Device will detect the rising edge of RST\_n signal to trigger internal reset sequence.

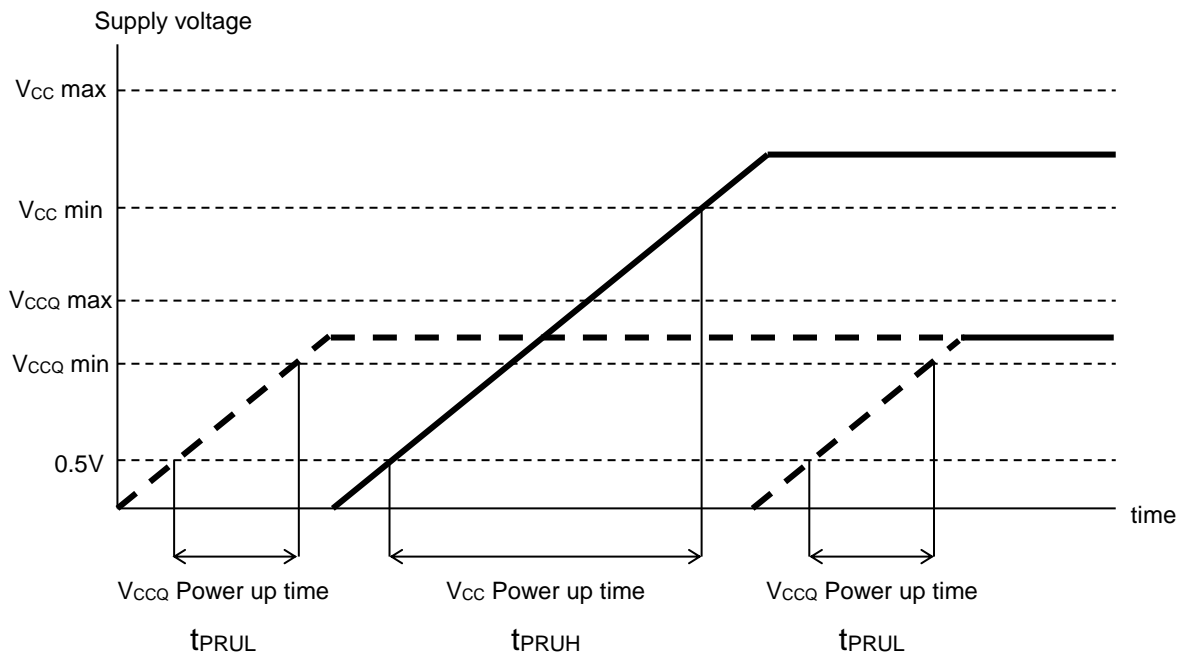
**H/W Reset Timings**

Symbol	Parameter	Min	Max	Unit
t <sub>RSTW</sub>	RST_n pulse width	1	—	μs
t <sub>RSCA</sub>	RST_n to Command time	200 <sup>Note 1</sup>	—	μs
t <sub>RSTH</sub>	RST_n high period (interval time)	1	—	μs

Note 1: 74 cycles of clock signal required before issuing CMD1 or CMD0 with argument 0xFFFFFFFF.

Note 2: During the device internal initialization sequence right after power on, device may not be able to detect RST\_n signal, because the device may not complete loading RST\_n\_ENABLE bits of the extended CSD register into the controller yet.

**Power-up sequence**



**Figure 5 Power up sequence**

**Power-up parameter**

Parameter	Symbol	Min	Max	Remark
Supply power-up for 3.3V	$t_{PRUH}$	5 $\mu$ s	35 ms	-
Supply power-up for 1.8V	$t_{PRUL}$	5 $\mu$ s	25 ms	-

### Functional restrictions

- Pre loading data size is limited to MAX\_PRE\_LOADING\_DATA\_SIZE[21-18] regardless of using Production State Awareness function.
- MAX\_PRE\_LOADING\_DATA\_SIZE[21-18] value will change when host sets Enhanced User area Partition.

### Reliability Guidance

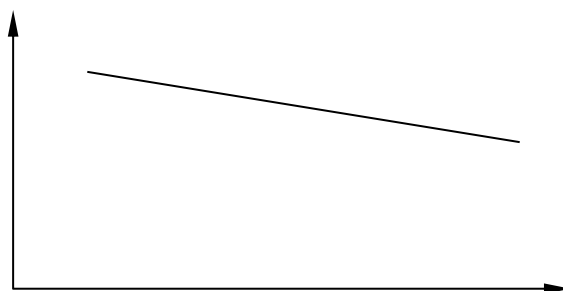
This reliability guidance is intended to notify some guidance related to using raw NAND flash. Although random bit errors may occur during use, it does not necessarily mean that a block is bad. Generally, a block should be marked as bad when a program status failure or erase status failure is detected. The other failure modes may be recovered by a block erase. ECC treatment for read data is mandatory due to the following Data Retention and Read Disturb failures.

#### -Write/Erase Endurance

Write/Erase endurance failures may occur in a cell, page, or block, and are detected by doing a status read after either an auto program or auto block erase operation. The cumulative bad block count will increase along with the number of write/erase cycles.

#### -Data Retention

The data in memory may change after a certain amount of storage time. This is due to charge loss or charge gain. After block erasure and reprogramming, the block may become usable again. Also write/erase endurance deteriorates data retention capability. The figure below shows a generic trend of relationship between write/erase endurance and data retention.



#### -Read Disturb

A read operation may disturb the data in memory. The data may change due to charge gain. Usually, bit errors occur on other pages in the block, not the page being read. After a large number of read cycles (between block erases), a tiny charge may build up and can cause a cell to be soft programmed to another state. After block erasure and reprogramming, the block may become usable again.

Considering the above failure modes, Toshiba Memory recommends following usage:

- Please avoid any excessive iteration of resets and initialization sequences (Device identification mode) as far as possible after power-on, which may result in read disturb failure. The resets include hardware resets and software resets.

e.g.1) Iteration of the following command sequence, CMD0 - CMD1 ---

The assertion of CMD1 implies a count of internal read operation in Raw NAND.

CMD0: Reset command, CMD1: Send operation command

e.g.2) Iteration of the following commands, CMD30 and/or CMD31

CMD30: Send status of write protection bits, CMD31: Send type of write protection

**Document Revision History**

Rev.0.1	February 13th, 2019	- Released as preliminary revision
Rev.0.2	February 14th, 2019	- Revised value of Operating Current (RMS) and Supply Current

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