



## SN74LVC1G32 Single 2-Input Positive-OR Gate

### 1 Features

- Available in the Ultra-Small 0.64 mm<sup>2</sup> Package (DPW) with 0.5-mm Pitch
- Supports 5-V V<sub>CC</sub> Operation
- Inputs Accept Voltages to 5.5-V
- Supports Down Translation to V<sub>CC</sub>
- Max t<sub>pd</sub> of 3.6 ns at 3.3-V
- Low Power Consumption, 10-μA Max I<sub>CC</sub>
- ±24-mA Output Drive at 3.3-V
- I<sub>off</sub> Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### 2 Applications

- AV Receiver
- Blu-ray Player and Home Theater
- Digital Picture Frame (DPF)
- Embedded PC
- IP Phone: Wireless
- High-Speed Data Acquisition and Generation
- Motor Control: High-Voltage
- Optical Networking: Video Over Fiber and EPON
- Personal Navigation Device (GPS)
- Portable Media Player
- Private Branch Exchange (PBX)
- Server PSU
- SSD: Internal and External
- TV: LCD/Digital and High-Definition (HDTV)
- Telecom Shelter: Power Distribution Unit (PDU), Power Monitoring Unit (PMU), Wireless Battery Monitoring, Remote Electrical Tilt Unit (RET), Remote Radio Unit (RRU), Tower Mounted Amplifier (TMA)
- Video Conferencing: IP-Based HD
- Vector Signal Analyzer and Generator
- WiMAX and Wireless Infrastructure Equipment
- Wireless Headset, Keyboard, Mouse, and Repeater

### 3 Description

This single 2-input positive-OR gate is designed for 1.65-V to 5.5-V V<sub>CC</sub> operation.

The SN74LVC1G32 device performs the Boolean function  $Y = A + B$  or  $Y = \overline{A} \cdot \overline{B}$  in positive logic.

The CMOS device has high output drive while maintaining low static power dissipation over a broad V<sub>CC</sub> operating range.

The SN74LVC1G32 device is available in a variety of packages, including the ultra-small DPW package with a body size of 0.8 × 0.8 mm.

Device Information<sup>(1)</sup>

| DEVICE NAME    | PACKAGE (PINS) | BODY SIZE         |
|----------------|----------------|-------------------|
| SN74LVC1G32DBV | SOT-23 (5)     | 2.90 mm × 2.80 mm |
| SN74LVC1G32DCK | SC70 (5)       | 2.00mm × 2.10 mm  |
| SN74LVC1G32DRY | SON (6)        | 1.45 mm × 1.00 mm |
| SN74LVC1G32DSF | SON (6)        | 1.00 mm × 1.00 mm |
| SN74LVC1G32DPW | X2SON (4)      | 0.80 mm × 0.80 mm |
| SN74LVC1G32DRL | SOT (5)        | 1.60 mm × 1.60 mm |
| SN74LVC1G32YZP | DSBGA (5)      | 1.38 mm × 0.88 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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## 4 Revision History

### Changes from Revision U (April 2014) to Revision V Page

|   |          |
|---|----------|
| • Added $T_J$ junction temp spec to Abs Max Ratings ..... | <b>5</b> |
|---|----------|

### Changes from Revision T (March 2014) to Revision U Page

|   |           |
|---|-----------|
| • Updated Features, Description, and Device Information table ..... | <b>1</b>  |
| • Added Pin Functions table. ....                                   | <b>4</b>  |
| • Added Thermal Information table. ....                             | <b>6</b>  |
| • Added Detailed Description section. ....                          | <b>11</b> |
| • Added Application and Implementation section. ....                | <b>12</b> |
| • Added Layout section. ....  | <b>13</b> |

### Changes from Revision S (July 2013) to Revision T Page

|   |          |
|---|----------|
| • Updated Features .....                          | <b>1</b> |
| • Added Applications .....                        | <b>1</b> |
| • Added Device Information table. ....            | <b>1</b> |
| • Added DPW Package. ....                         | <b>4</b> |
| • Moved $T_{stg}$ to Handling Ratings table. .... | <b>5</b> |

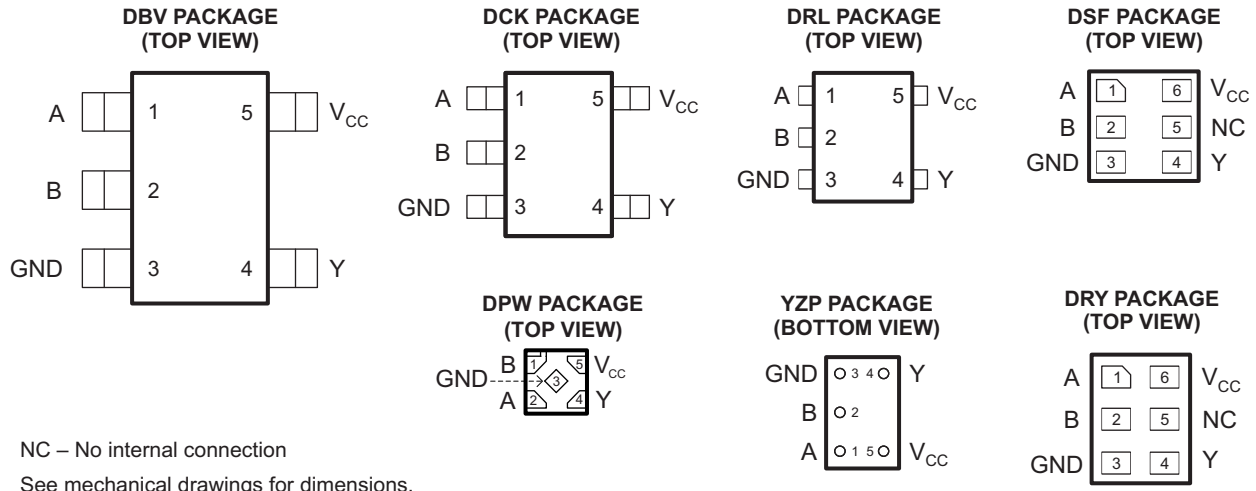
### Changes from Revision R (June 2013) to Revision S Page

|   |          |
|---|----------|
| • Added parameter values for –40 to 125°C temperature ratings ..... | <b>7</b> |
|---|----------|

**Changes from Revision Q (November 2012) to Revision R****Page**

- 
- Deleted Ordering Information table. .... [1](#)
-

## 5 Pin Configuration and Functions



### Pin Functions

| NAME            | PIN                |          |     | DESCRIPTION   |
|-----------------|--------------------|----------|-----|---------------|
|                 | DBV, DCK, DRL, YZP | DRY, DSF | DPW |               |
| A               | 1                  | 1        | 2   | Input         |
| B               | 2                  | 2        | 1   | Input         |
| GND             | 3                  | 3        | 3   | Ground        |
| Y               | 4                  | 4        | 4   | Output        |
| V <sub>CC</sub> | 5                  | 6        | 5   | Power pin     |
| NC              | –                  | 5        | –   | Not connected |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                  |   | MIN                | MAX                   | UNIT |
|------------------|---|--------------------|-----------------------|------|
| V <sub>CC</sub>  | Supply voltage range  | –0.5               | 6.5                   | V    |
| V <sub>I</sub>   | Input voltage range <sup>(2)</sup>  | –0.5               | 6.5                   | V    |
| V <sub>O</sub>   | Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup> | –0.5               | 6.5                   | V    |
| V <sub>O</sub>   | Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>              | –0.5               | V <sub>CC</sub> + 0.5 | V    |
| I <sub>IK</sub>  | Input clamp current   | V <sub>I</sub> < 0 | –50                   | mA   |
| I <sub>OK</sub>  | Output clamp current  | V <sub>O</sub> < 0 | –50                   | mA   |
| I <sub>O</sub>   | Continuous output current   |                    | ±50                   | mA   |
|                  | Continuous current through V <sub>CC</sub> or GND   |                    | ±100                  | mA   |
| T <sub>J</sub>   | Junction temperature  | –65                | 150                   | °C   |
| T <sub>stg</sub> | Storage temperature   | –65                | 150                   | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the *Recommended Operating Conditions* table.

### 6.2 ESD Ratings

| PARAMETER          | DEFINITION              | VALUE  | UNIT |
|--------------------|-------------------------|--|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>              | V    |
|                    |                         | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup> |      |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                                    |   | MIN                    | MAX                    | UNIT |
|-----------------|------------------------------------|---|------------------------|------------------------|------|
| V <sub>CC</sub> | Supply voltage                     | Operating                                       | 1.65                   | 5.5                    | V    |
|                 |                                    | Data retention only                             | 1.5                    |                        |      |
| V <sub>IH</sub> | High-level input voltage           | V <sub>CC</sub> = 1.65 V to 1.95 V              | 0.65 × V <sub>CC</sub> |                        | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V                | 1.7                    |                        |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V                  | 2                      |                        |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V                | 0.7 × V <sub>CC</sub>  |                        |      |
| V <sub>IL</sub> | Low-level input voltage            | V <sub>CC</sub> = 1.65 V to 1.95 V              |                        | 0.35 × V <sub>CC</sub> | V    |
|                 |                                    | V <sub>CC</sub> = 2.3 V to 2.7 V                |                        | 0.7                    |      |
|                 |                                    | V <sub>CC</sub> = 3 V to 3.6 V                  |                        | 0.8                    |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V to 5.5 V                |                        | 0.3 × V <sub>CC</sub>  |      |
| V <sub>I</sub>  | Input voltage                      |   | 0                      | 5.5                    | V    |
| V <sub>O</sub>  | Output voltage                     |   | 0                      | V <sub>CC</sub>        | V    |
| I <sub>OH</sub> | High-level output current          | V <sub>CC</sub> = 1.65 V                        |                        | –4                     | mA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V                         |                        | –8                     |      |
|                 |                                    | V <sub>CC</sub> = 3 V                           |                        | –16                    |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V                         |                        | –24                    |      |
| I <sub>OL</sub> | Low-level output current           | V <sub>CC</sub> = 1.65 V                        |                        | 4                      | mA   |
|                 |                                    | V <sub>CC</sub> = 2.3 V                         |                        | 8                      |      |
|                 |                                    | V <sub>CC</sub> = 3 V                           |                        | 16                     |      |
|                 |                                    | V <sub>CC</sub> = 4.5 V                         |                        | 24                     |      |
| Δt/Δv           | Input transition rise or fall rate | V <sub>CC</sub> = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V |                        | 20                     | ns/V |
|                 |                                    | V <sub>CC</sub> = 3.3 V ± 0.3 V                 |                        | 10                     |      |
|                 |                                    | V <sub>CC</sub> = 5 V ± 0.5 V                   |                        | 5                      |      |
| T <sub>A</sub>  | Operating free-air temperature     | DSBGA package                                   | –40                    | 85                     | °C   |
|                 |                                    | All other packages                              | –40                    | 125                    | °C   |

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

### 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> | SN74LVC1G32                                  |        |        |        |        |        | UNIT |      |
|-------------------------------|--|--------|--------|--------|--------|--------|------|------|
|                               | DBV  | DCK    | DRL    | DRY    | YZP    | DPW    |      |      |
|                               | 5 PINS                                       | 5 PINS | 5 PINS | 6 PINS | 5 PINS | 4 PINS |      |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 229    | 278    | 243    | 439    | 130    | 340  | °C/W |
| R <sub>θJctop</sub>           | Junction-to-case (top) thermal resistance    | 164    | 93     | 78     | 277    | 54     | 215  |      |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 62     | 65     | 78     | 271    | 51     | 294  |      |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 44     | 2      | 10     | 84     | 1      | 41   |      |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 62     | 64     | 77     | 271    | 50     | 294  |      |
| R <sub>θJcbot</sub>           | Junction-to-case (bottom) thermal resistance | –      | –      | –      | –      | –      | 250  |      |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report ([SPRA953](#)).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER        | TEST CONDITIONS           | V <sub>CC</sub>   | –40°C to 85°C         |                    |     | –40°C to 125°C RECOMMENDED |     |     | UNIT |
|------------------|---------------------------|---|-----------------------|--------------------|-----|----------------------------|-----|-----|------|
|                  |                           |   | MIN                   | TYP <sup>(1)</sup> | MAX | MIN                        | TYP | MAX |      |
| V <sub>OH</sub>  | I <sub>OH</sub> = –100 μA | 1.65 V to 5.5 V   | V <sub>CC</sub> – 0.1 |                    |     | V <sub>CC</sub> – 0.1      |     |     | V    |
|                  | I <sub>OH</sub> = –4 mA   | 1.65 V  | 1.2                   |                    |     | 1.2                        |     |     |      |
|                  | I <sub>OH</sub> = –8 mA   | 2.3 V   | 1.9                   |                    |     | 1.9                        |     |     |      |
|                  | I <sub>OH</sub> = –16 mA  | 3 V   | 2.4                   |                    |     | 2.4                        |     |     |      |
|                  | I <sub>OH</sub> = –24 mA  |   | 2.3                   |                    |     | 2.3                        |     |     |      |
|                  | I <sub>OH</sub> = –32 mA  | 4.5 V   | 3.8                   |                    |     | 3.8                        |     |     |      |
| V <sub>OL</sub>  | I <sub>OL</sub> = 100 μA  | 1.65 V to 5.5 V   | 0.1                   |                    |     | 0.1                        |     |     | V    |
|                  | I <sub>OL</sub> = 4 mA    | 1.65 V  | 0.45                  |                    |     | 0.45                       |     |     |      |
|                  | I <sub>OL</sub> = 8 mA    | 2.3 V   | 0.3                   |                    |     | 0.4                        |     |     |      |
|                  | I <sub>OL</sub> = 16 mA   | 3 V   | 0.4                   |                    |     | 0.5                        |     |     |      |
|                  | I <sub>OL</sub> = 24 mA   |   | 0.55                  |                    |     | 0.65                       |     |     |      |
|                  | I <sub>OL</sub> = 32 mA   | 4.5 V   | 0.55                  |                    |     | 0.65                       |     |     |      |
| I <sub>I</sub>   | A or B inputs             | V <sub>I</sub> = 5.5 V or GND   | 0 to 5.5 V            |                    |     | ±5                         |     |     | μA   |
| I <sub>off</sub> |                           | V <sub>I</sub> or V <sub>O</sub> = 5.5 V  | 0                     |                    |     | ±10                        |     |     | μA   |
| I <sub>CC</sub>  |                           | V <sub>I</sub> = 5.5 V or GND, I <sub>O</sub> = 0                               | 1.65 V to 5.5 V       |                    |     | 10                         |     |     | μA   |
| ΔI <sub>CC</sub> |                           | One input at V <sub>CC</sub> – 0.6 V,<br>Other inputs at V <sub>CC</sub> or GND | 3 V to 5.5 V          |                    |     | 500                        |     |     | μA   |
| C <sub>i</sub>   |                           | V <sub>I</sub> = V <sub>CC</sub> or GND   | 3.3 V                 |                    |     | 4                          |     |     | pF   |

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## 6.6 Switching Characteristics, C<sub>L</sub> = 15 pF

over recommended operating free-air temperature range, C<sub>L</sub> = 15 pF (unless otherwise noted) (see Figure 3)

| PARAMETER       | FROM (INPUT) | TO (OUTPUT) | –40°C to 85°C                    |     |                                 |     |                                 |     |                               |     | UNIT |
|-----------------|--------------|-------------|----------------------------------|-----|---------------------------------|-----|---------------------------------|-----|-------------------------------|-----|------|
|                 |              |             | V <sub>CC</sub> = 1.8 V ± 0.15 V |     | V <sub>CC</sub> = 2.5 V ± 0.2 V |     | V <sub>CC</sub> = 3.3 V ± 0.3 V |     | V <sub>CC</sub> = 5 V ± 0.5 V |     |      |
|                 |              |             | MIN                              | MAX | MIN                             | MAX | MIN                             | MAX | MIN                           | MAX |      |
| t <sub>pd</sub> | A or B       | Y           | 1.9                              | 7.2 | 0.8                             | 4.4 | 0.9                             | 3.6 | 0.8                           | 3.4 | ns   |

## 6.7 Switching Characteristics, 1.8 V and 2.5V

over recommended operating free-air temperature range, C<sub>L</sub> = 30 pF or 50 pF (unless otherwise noted)<sup>(1)</sup> (see Figure 4)

| PARAMETER       | FROM (INPUT) | TO (OUTPUT) | –40°C to 85°C                    |     | –40°C to 125°C RECOMMENDED       |     | –40°C to 85°C                   |     | –40°C to 125°C RECOMMENDED      |     | UNIT |
|-----------------|--------------|-------------|----------------------------------|-----|----------------------------------|-----|---------------------------------|-----|---------------------------------|-----|------|
|                 |              |             | V <sub>CC</sub> = 1.8 V ± 0.15 V |     | V <sub>CC</sub> = 1.8 V ± 0.15 V |     | V <sub>CC</sub> = 2.5 V ± 0.2 V |     | V <sub>CC</sub> = 2.5 V ± 0.2 V |     |      |
|                 |              |             | MIN                              | MAX | MIN                              | MAX | MIN                             | MAX | MIN                             | MAX |      |
| t <sub>pd</sub> | A or B       | Y           | 2.8                              | 8   | 2.8                              | 9   | 1.2                             | 5.5 | 1.2                             | 6   | ns   |

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

### 6.8 Switching Characteristics, 3.3 V and 5 V

over recommended operating free-air temperature range,  $C_L = 30\text{ pF}$  or  $50\text{ pF}$  (unless otherwise noted)<sup>(1)</sup> (see Figure 4)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | -40°C to 85°C                            |     | -40°C to 125°C RECOMMENDED               |     | -40°C to 85°C                          |     | -40°C to 125°C RECOMMENDED             |     | UNIT |
|-----------|--------------|-------------|--|-----|--|-----|--|-----|--|-----|------|
|           |              |             | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |     | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ |     | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ |     |      |
|           |              |             | MIN                                      | MAX | MIN                                      | MAX | MIN                                    | MAX | MIN                                    | MAX |      |
| $t_{pd}$  | A or B       | Y           | 1.1                                      | 4.5 | 1  | 4   | 1                                      | 4   | 1                                      | 4.5 | ns   |

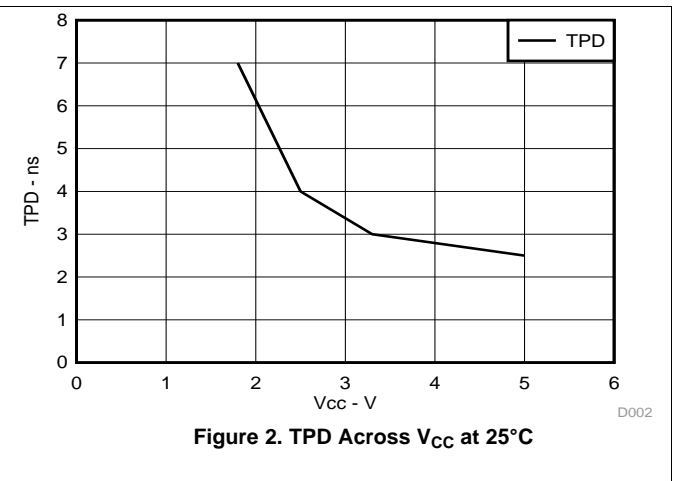
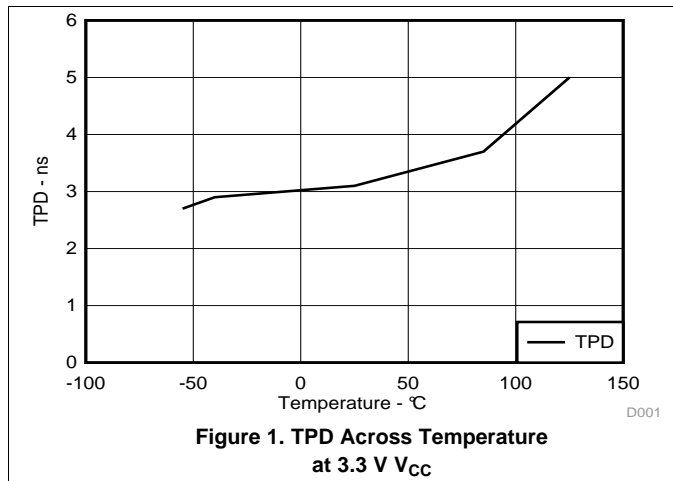
(1) On products compliant to MIL-PRF-38535, this parameter is not production tested

### 6.9 Operating Characteristics

$T_A = 25^\circ\text{C}$

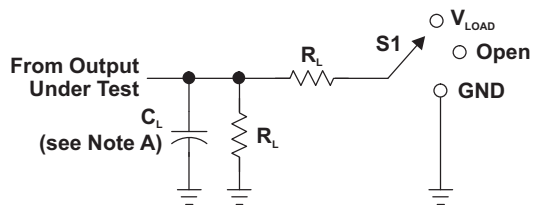
| PARAMETER                              | TEST CONDITIONS     | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | $V_{CC} = 5\text{ V}$ | UNIT |
|--|---------------------|-------------------------|-------------------------|-------------------------|-----------------------|------|
|  |                     | TYP                     | TYP                     | TYP                     | TYP                   |      |
| $C_{pd}$ Power dissipation capacitance | $f = 10\text{ MHz}$ | 20                      | 20                      | 21                      | 22                    | pF   |

### 6.10 Typical Characteristics





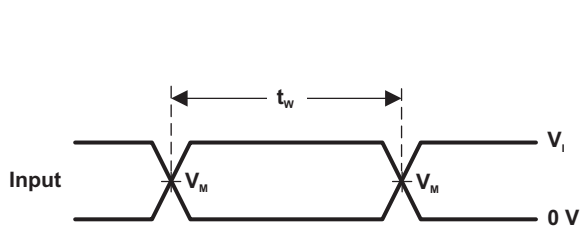
## 7 Parameter Measurement Information



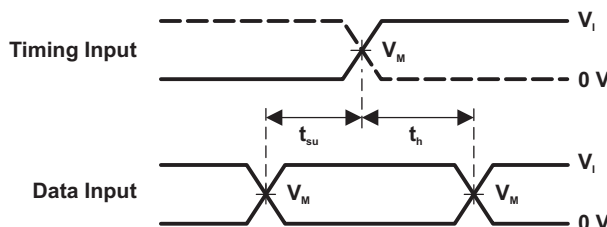
LOAD CIRCUIT

| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

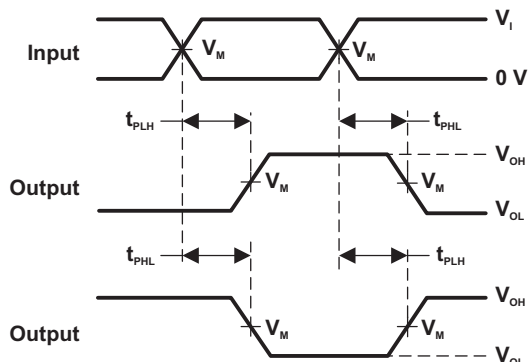
| $V_{CC}$                         | INPUTS   |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_i$    | $t_i/t_r$            |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M $\Omega$ | 0.15 V       |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M $\Omega$ | 0.15 V       |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 3 V      | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 15 pF | 1 M $\Omega$ | 0.3 V        |
| $5\text{ V} \pm 0.5\text{ V}$    | $V_{CC}$ | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 15 pF | 1 M $\Omega$ | 0.3 V        |



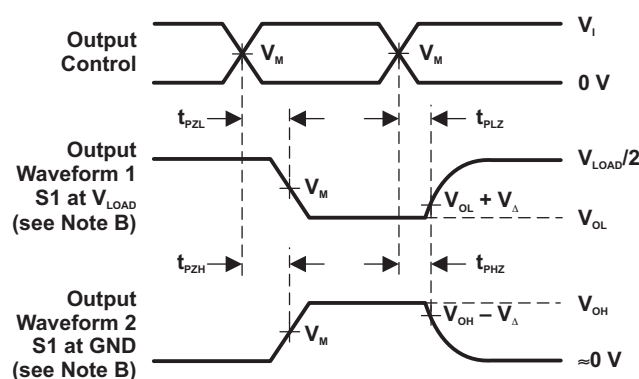
VOLTAGE WAVEFORMS PULSE DURATION



VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



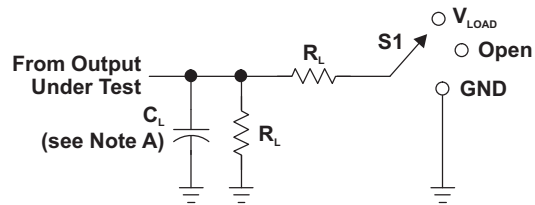
VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES LOW- AND HIGH-LEVEL ENABLING

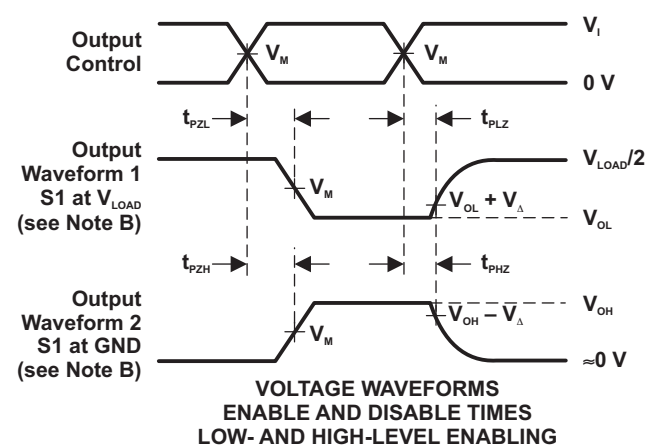
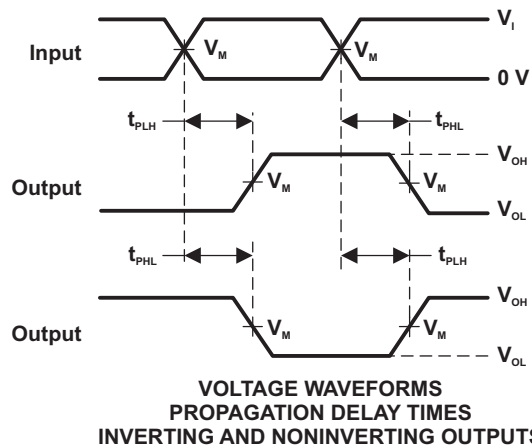
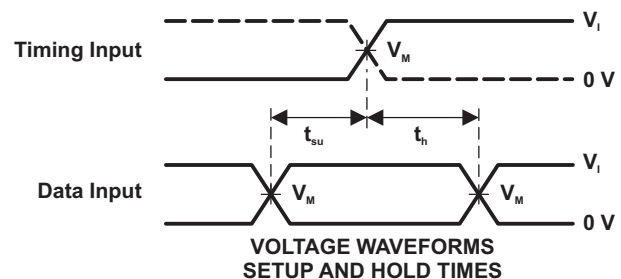
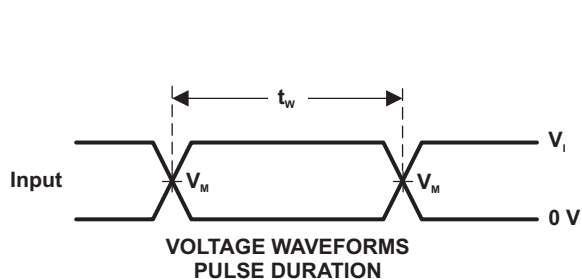
- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_o = 50\ \Omega$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

**Parameter Measurement Information (continued)**

**LOAD CIRCUIT**

| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

| $V_{CC}$                         | INPUTS   |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_I$    | $t_r/t_f$            |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k $\Omega$ | 0.15 V       |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 3 V      | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |
| $5\text{ V} \pm 0.5\text{ V}$    | $V_{CC}$ | $\leq 2.5\text{ ns}$ | $V_{CC}/2$ | $2 \times V_{CC}$ | 50 pF | 500 $\Omega$ | 0.3 V        |



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_o = 50\ \Omega$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{on}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

**Figure 4. Load Circuit and Voltage Waveforms**

## 8 Detailed Description

### 8.1 Overview

The SN74LVC1G32 device contains one 2-input positive OR gate device and performs the Boolean function  $Y = A + B$  or  $Y = \overline{A \cdot B}$ . This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The DPW package technology is a major breakthrough in IC packaging. Its tiny 0.64 mm square footprint saves significant board space over other package options while still retaining the traditional manufacturing friendly lead pitch of 0.5 mm.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

- Wide operating voltage range.
  - Operates from 1.65 V to 5.5 V.
- Allows down voltage translation.
- Inputs accept voltages to 5.5 V.
- $I_{off}$  feature allows voltages on the inputs and outputs, when  $V_{CC}$  is 0 V.

### 8.4 Device Functional Modes

Function Table

| INPUTS |   | OUTPUT<br>Y |
|--------|---|-------------|
| A      | B |             |
| H      | X | H           |
| X      | H | H           |
| L      | L | L           |

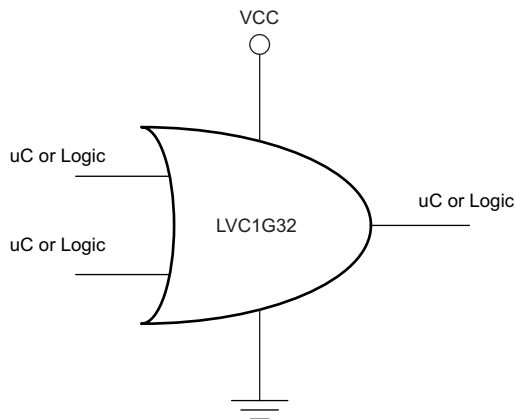
## 9 Application and Implementation

### 9.1 Application Information

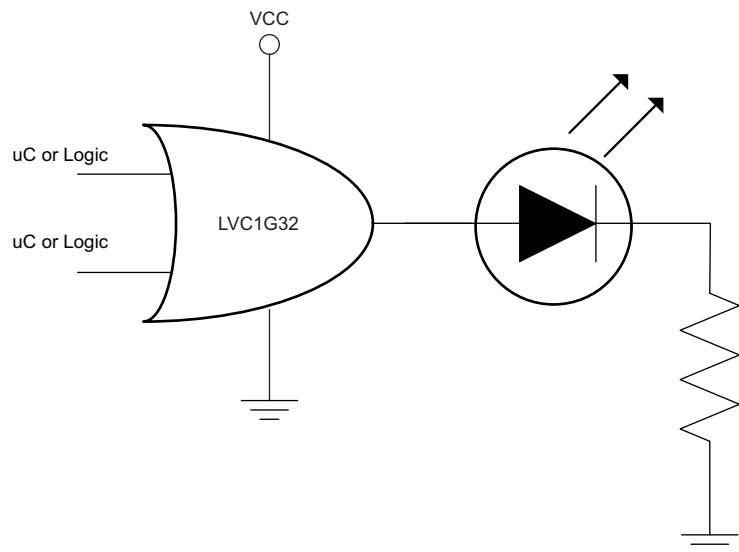
The SN74LVC1G32 device is a high drive CMOS device that can be used for implementing OR logic with a high output drive, such as an LED application. It can produce 24 mA of drive current at 3.3 V making it ideal for driving multiple outputs and good for high speed applications up to 100 MHz. The inputs are 5.5-V tolerant allowing translation down to  $V_{CC}$ .

### 9.2 Typical Application

OR Logic Function



Basic LED Driver



#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads, so routing and load conditions should be considered to prevent ringing.

#### 9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
  - Rise time and fall time specs. See  $(\Delta t/\Delta V)$  in the [Recommended Operating Conditions](#) table.
  - Specified high and low levels. See  $(V_{IH}$  and  $V_{IL})$  in the [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as  $(V_I \text{ max})$  in the [Recommended Operating Conditions](#) table at any valid  $V_{CC}$ .
2. Recommended Output Conditions:
  - Load currents should not exceed  $(I_O \text{ max})$  per output and should not exceed total current (continuous current through  $V_{CC}$  or GND) for the part. These limits are located in the [Absolute Maximum Ratings](#) table.
  - Outputs should not be pulled above  $V_{CC}$ .

## Typical Application (continued)

### 9.2.3 Application Curves

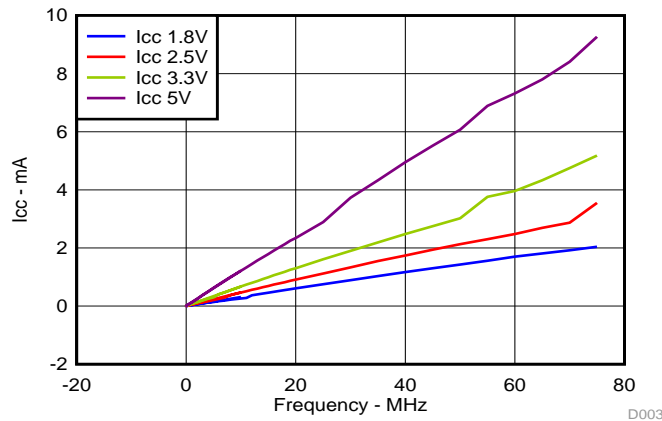


Figure 5. I<sub>CC</sub> vs Frequency

## 10 Power Supply Recommendations

The power supply can be any voltage between the min and max supply voltage rating located in the [Recommended Operating Conditions](#) table.

Each VCC pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1- $\mu$ F capacitor is recommended. If there are multiple VCC pins, then a 0.01- $\mu$ F or 0.022- $\mu$ F capacitor is recommended for each power pin. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

## 11 Layout

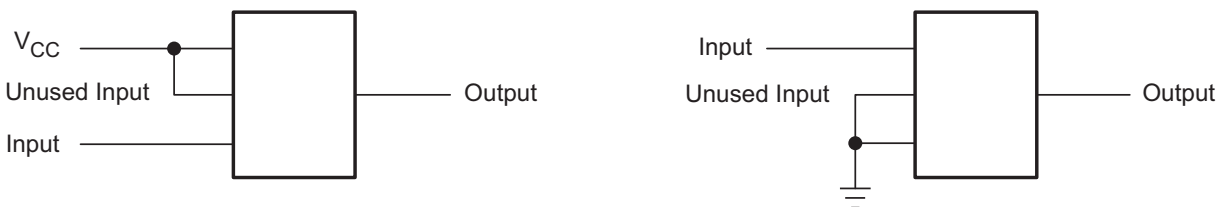
### 11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used, or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Layout Example](#) are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or VCC, whichever make more sense or is more convenient.

### 11.2 Layout Example



## 12 Device and Documentation Support

### 12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.2 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

| Orderable Device  | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)     | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)                                 | Samples                 |
|-------------------|---------------|--------------|-----------------|------|-------------|---------------------|--------------------------------------|----------------------|--------------|---|-------------------------|
| SN74LVC1G32DBVR   | ACTIVE        | SOT-23       | DBV             | 5    | 3000        | RoHS & Green        | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 125   | (C325, C32F, C32J,<br>C32K, C32R)<br>(C32H, C32P, C32S) | <a href="#">Samples</a> |
| SN74LVC1G32DBVRE4 | ACTIVE        | SOT-23       | DBV             | 5    | 3000        | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | C32F  | <a href="#">Samples</a> |
| SN74LVC1G32DBVRG4 | ACTIVE        | SOT-23       | DBV             | 5    | 3000        | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | C32F  | <a href="#">Samples</a> |
| SN74LVC1G32DBVT   | ACTIVE        | SOT-23       | DBV             | 5    | 250         | RoHS & Green        | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 125   | (C325, C32F, C32J,<br>C32K, C32R)<br>(C32H, C32P, C32S) | <a href="#">Samples</a> |
| SN74LVC1G32DBVTG4 | ACTIVE        | SOT-23       | DBV             | 5    | 250         | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | C32F  | <a href="#">Samples</a> |
| SN74LVC1G32DCK3   | ACTIVE        | SC70         | DCK             | 5    | 3000        | RoHS &<br>Non-Green | SNBI                                 | Level-1-260C-UNLIM   | -40 to 125   | (CGF, CGZ)  | <a href="#">Samples</a> |
| SN74LVC1G32DCKR   | ACTIVE        | SC70         | DCK             | 5    | 3000        | RoHS & Green        | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 125   | (CG5, CGF, CGJ, CG<br>K, CGR)<br>(CGH, CGP, CGS)        | <a href="#">Samples</a> |
| SN74LVC1G32DCKRE4 | ACTIVE        | SC70         | DCK             | 5    | 3000        | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | CG5<br>CGS  | <a href="#">Samples</a> |
| SN74LVC1G32DCKRG4 | ACTIVE        | SC70         | DCK             | 5    | 3000        | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | CG5<br>CGS  | <a href="#">Samples</a> |
| SN74LVC1G32DCKT   | ACTIVE        | SC70         | DCK             | 5    | 250         | RoHS & Green        | NIPDAU   SN                          | Level-1-260C-UNLIM   | -40 to 125   | (CG5, CGF, CGJ, CG<br>K, CGR)<br>(CGH, CGP, CGS)        | <a href="#">Samples</a> |
| SN74LVC1G32DCKTG4 | ACTIVE        | SC70         | DCK             | 5    | 250         | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | CG5<br>CGS  | <a href="#">Samples</a> |
| SN74LVC1G32DPWR   | ACTIVE        | X2SON        | DPW             | 5    | 3000        | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | N4  | <a href="#">Samples</a> |
| SN74LVC1G32DRLR   | ACTIVE        | SOT-5X3      | DRL             | 5    | 4000        | RoHS & Green        | NIPDAUAG                             | Level-1-260C-UNLIM   | -40 to 125   | (CG7, CGR)  | <a href="#">Samples</a> |
| SN74LVC1G32DRLRG4 | ACTIVE        | SOT-5X3      | DRL             | 5    | 4000        | RoHS & Green        | NIPDAUAG                             | Level-1-260C-UNLIM   | -40 to 125   | (CG7, CGR)  | <a href="#">Samples</a> |
| SN74LVC1G32DRY2   | ACTIVE        | SON          | DRY             | 6    | 5000        | RoHS & Green        | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | CG  | <a href="#">Samples</a> |

| Orderable Device | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| SN74LVC1G32DRYR  | ACTIVE        | SON          | DRY             | 6    | 5000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | CG                      | <a href="#">Samples</a> |
| SN74LVC1G32DSF2  | ACTIVE        | SON          | DSF             | 6    | 5000        | RoHS & Green    | NIPDAU                               | Level-1-260C-UNLIM   | -40 to 125   | CG                      | <a href="#">Samples</a> |
| SN74LVC1G32DSFR  | ACTIVE        | SON          | DSF             | 6    | 5000        | RoHS & Green    | NIPDAU   NIPDAUAG                    | Level-1-260C-UNLIM   | -40 to 125   | CG                      | <a href="#">Samples</a> |
| SN74LVC1G32YZPR  | ACTIVE        | DSBGA        | YZP             | 5    | 3000        | RoHS & Green    | SNAGCU                               | Level-1-260C-UNLIM   | -40 to 85    | (CG, CG7)               | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74LVC1G32 :**

- Automotive : [SN74LVC1G32-Q1](#)
- Enhanced Product : [SN74LVC1G32-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC1G32DBVR   | SOT-23       | DBV             | 5    | 3000 | 180.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| SN74LVC1G32DBVRG4 | SOT-23       | DBV             | 5    | 3000 | 178.0              | 9.0                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| SN74LVC1G32DBVT   | SOT-23       | DBV             | 5    | 250  | 180.0              | 8.4                | 3.2     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| SN74LVC1G32DBVTG4 | SOT-23       | DBV             | 5    | 250  | 178.0              | 9.0                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| SN74LVC1G32DCKR   | SC70         | DCK             | 5    | 3000 | 178.0              | 9.0                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| SN74LVC1G32DCKR   | SC70         | DCK             | 5    | 3000 | 178.0              | 9.2                | 2.4     | 2.4     | 1.22    | 4.0     | 8.0    | Q3            |
| SN74LVC1G32DCKRG4 | SC70         | DCK             | 5    | 3000 | 178.0              | 9.2                | 2.4     | 2.4     | 1.22    | 4.0     | 8.0    | Q3            |
| SN74LVC1G32DCKT   | SC70         | DCK             | 5    | 250  | 178.0              | 9.0                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |
| SN74LVC1G32DCKT   | SC70         | DCK             | 5    | 250  | 180.0              | 8.4                | 2.47    | 2.3     | 1.25    | 4.0     | 8.0    | Q3            |
| SN74LVC1G32DCKT   | SC70         | DCK             | 5    | 250  | 178.0              | 9.2                | 2.4     | 2.4     | 1.22    | 4.0     | 8.0    | Q3            |
| SN74LVC1G32DCKTG4 | SC70         | DCK             | 5    | 250  | 178.0              | 9.2                | 2.4     | 2.4     | 1.22    | 4.0     | 8.0    | Q3            |
| SN74LVC1G32DPWR   | X2SON        | DPW             | 5    | 3000 | 178.0              | 8.4                | 0.91    | 0.91    | 0.5     | 2.0     | 8.0    | Q3            |
| SN74LVC1G32DRLR   | SOT-5X3      | DRL             | 5    | 4000 | 180.0              | 8.4                | 1.98    | 1.78    | 0.69    | 4.0     | 8.0    | Q3            |
| SN74LVC1G32DRY2   | SON          | DRY             | 6    | 5000 | 180.0              | 9.5                | 1.6     | 1.15    | 0.75    | 4.0     | 8.0    | Q3            |
| SN74LVC1G32DRYR   | SON          | DRY             | 6    | 5000 | 180.0              | 9.5                | 1.15    | 1.6     | 0.75    | 4.0     | 8.0    | Q1            |
| SN74LVC1G32DSF2   | SON          | DSF             | 6    | 5000 | 180.0              | 9.5                | 1.16    | 1.16    | 0.5     | 4.0     | 8.0    | Q3            |

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVC1G32DSFR | SON          | DSF             | 6    | 5000 | 180.0              | 8.4                | 1.16    | 1.16    | 0.63    | 4.0     | 8.0    | Q2            |
| SN74LVC1G32DSFR | SON          | DSF             | 6    | 5000 | 180.0              | 9.5                | 1.16    | 1.16    | 0.5     | 4.0     | 8.0    | Q2            |
| SN74LVC1G32YZPR | DSBGA        | YZP             | 5    | 3000 | 180.0              | 8.4                | 1.02    | 1.52    | 0.63    | 4.0     | 8.0    | Q1            |

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device            | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC1G32DBVR   | SOT-23       | DBV             | 5    | 3000 | 210.0       | 185.0      | 35.0        |
| SN74LVC1G32DBVRG4 | SOT-23       | DBV             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74LVC1G32DBVT   | SOT-23       | DBV             | 5    | 250  | 210.0       | 185.0      | 35.0        |
| SN74LVC1G32DBVTG4 | SOT-23       | DBV             | 5    | 250  | 180.0       | 180.0      | 18.0        |
| SN74LVC1G32DCKR   | SC70         | DCK             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74LVC1G32DCKR   | SC70         | DCK             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74LVC1G32DCKRG4 | SC70         | DCK             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74LVC1G32DCKT   | SC70         | DCK             | 5    | 250  | 180.0       | 180.0      | 18.0        |
| SN74LVC1G32DCKT   | SC70         | DCK             | 5    | 250  | 202.0       | 201.0      | 28.0        |
| SN74LVC1G32DCKT   | SC70         | DCK             | 5    | 250  | 180.0       | 180.0      | 18.0        |
| SN74LVC1G32DCKTG4 | SC70         | DCK             | 5    | 250  | 180.0       | 180.0      | 18.0        |
| SN74LVC1G32DPWR   | X2SON        | DPW             | 5    | 3000 | 205.0       | 200.0      | 33.0        |
| SN74LVC1G32DRLR   | SOT-5X3      | DRL             | 5    | 4000 | 202.0       | 201.0      | 28.0        |
| SN74LVC1G32DRY2   | SON          | DRY             | 6    | 5000 | 184.0       | 184.0      | 19.0        |
| SN74LVC1G32DRYR   | SON          | DRY             | 6    | 5000 | 184.0       | 184.0      | 19.0        |
| SN74LVC1G32DSF2   | SON          | DSF             | 6    | 5000 | 184.0       | 184.0      | 19.0        |
| SN74LVC1G32DSFR   | SON          | DSF             | 6    | 5000 | 202.0       | 201.0      | 28.0        |
| SN74LVC1G32DSFR   | SON          | DSF             | 6    | 5000 | 184.0       | 184.0      | 19.0        |

---

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVC1G32YZPR | DSBGA        | YZP             | 5    | 3000 | 182.0       | 182.0      | 20.0        |

## GENERIC PACKAGE VIEW

DPW 5

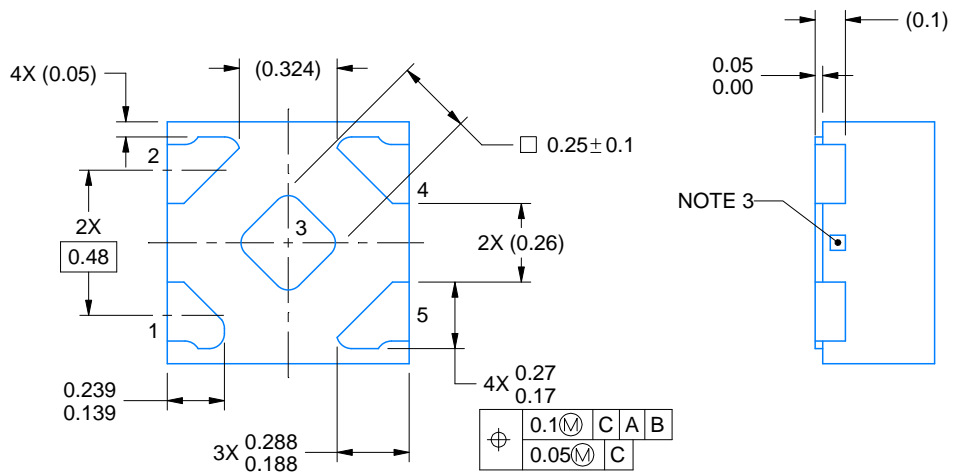
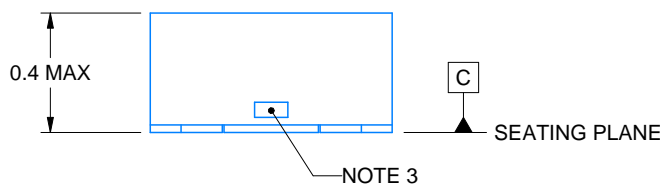
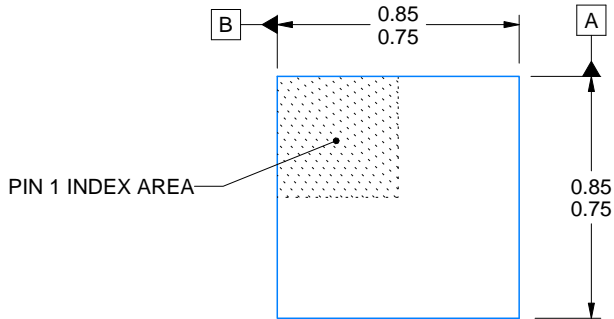
X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4211218-3/D



4223102/D 03/2022

NOTES:

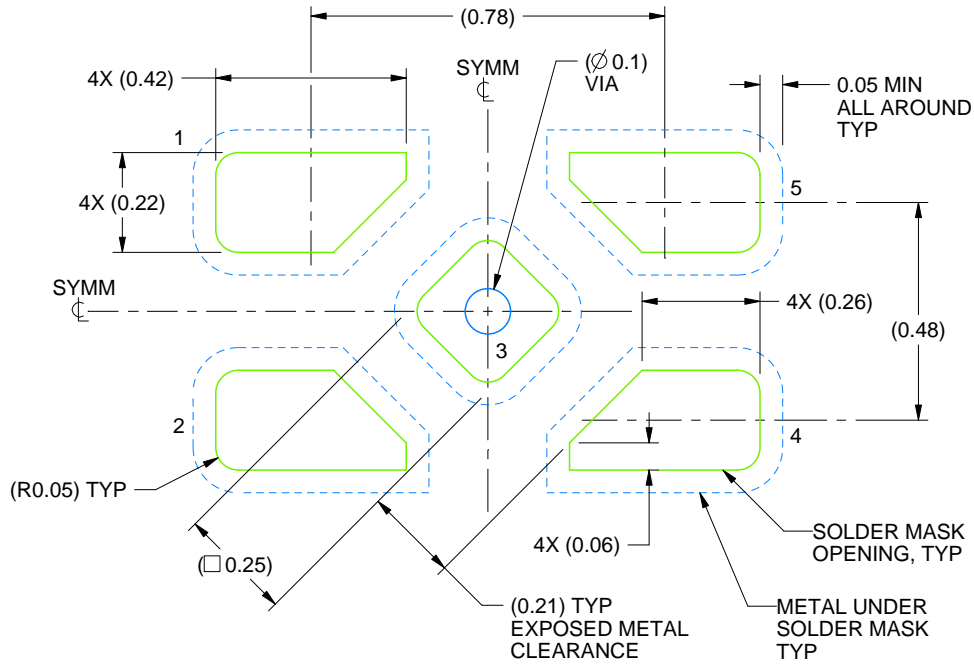
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.

# EXAMPLE BOARD LAYOUT

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SOLDER MASK DEFINED  
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 ([www.ti.com/lit/sl原因271](http://www.ti.com/lit/sl原因271)).



# EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3  
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:100X

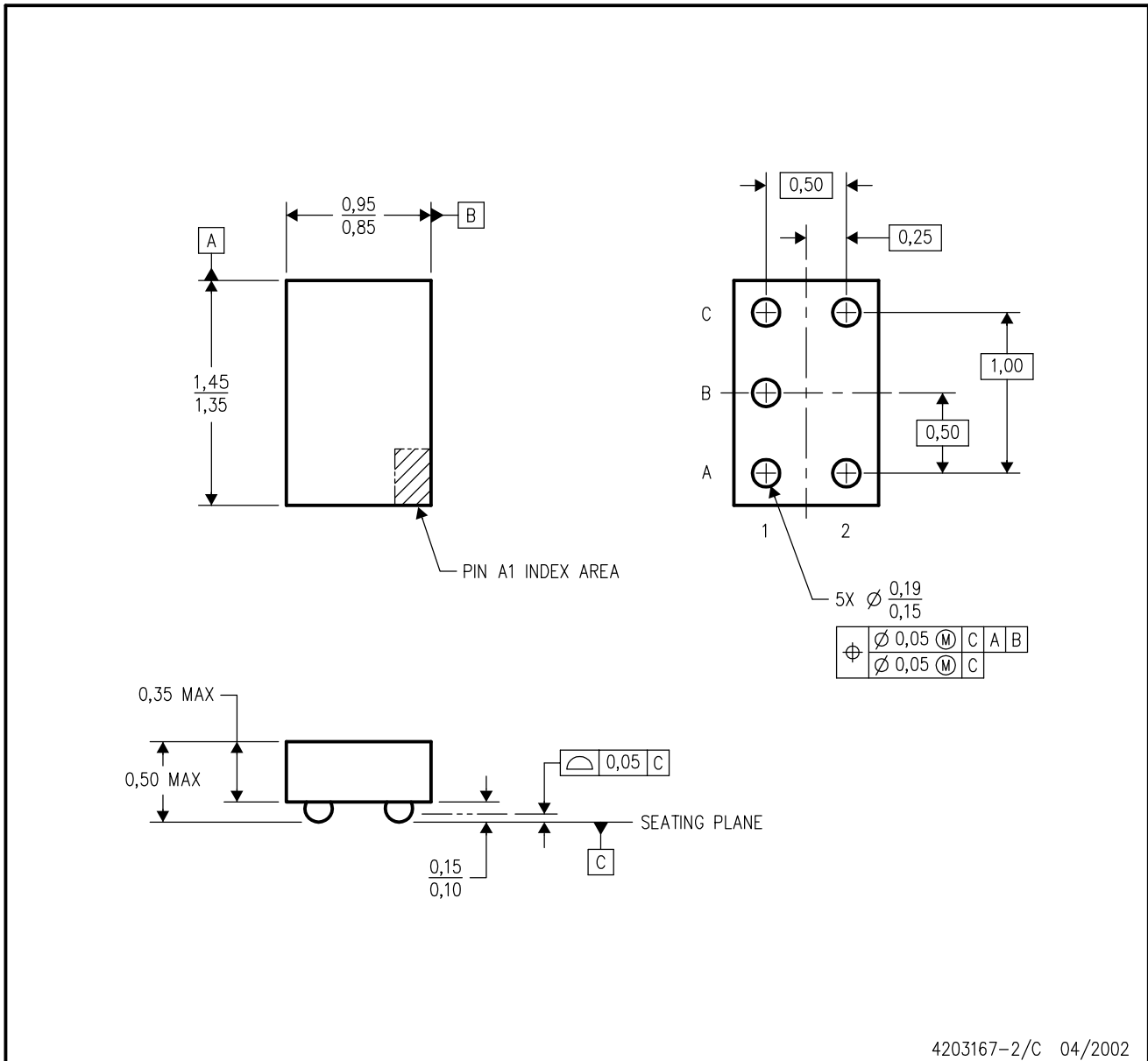
4223102/D 03/2022

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

YEA (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. NanoStar™ package configuration.
  - D. Package complies to JEDEC MO-211 variation EA.
  - E. This package is tin-lead (SnPb). Refer to the 5 YZA package (drawing 4204151) for lead-free.

NanoStar is a trademark of Texas Instruments.

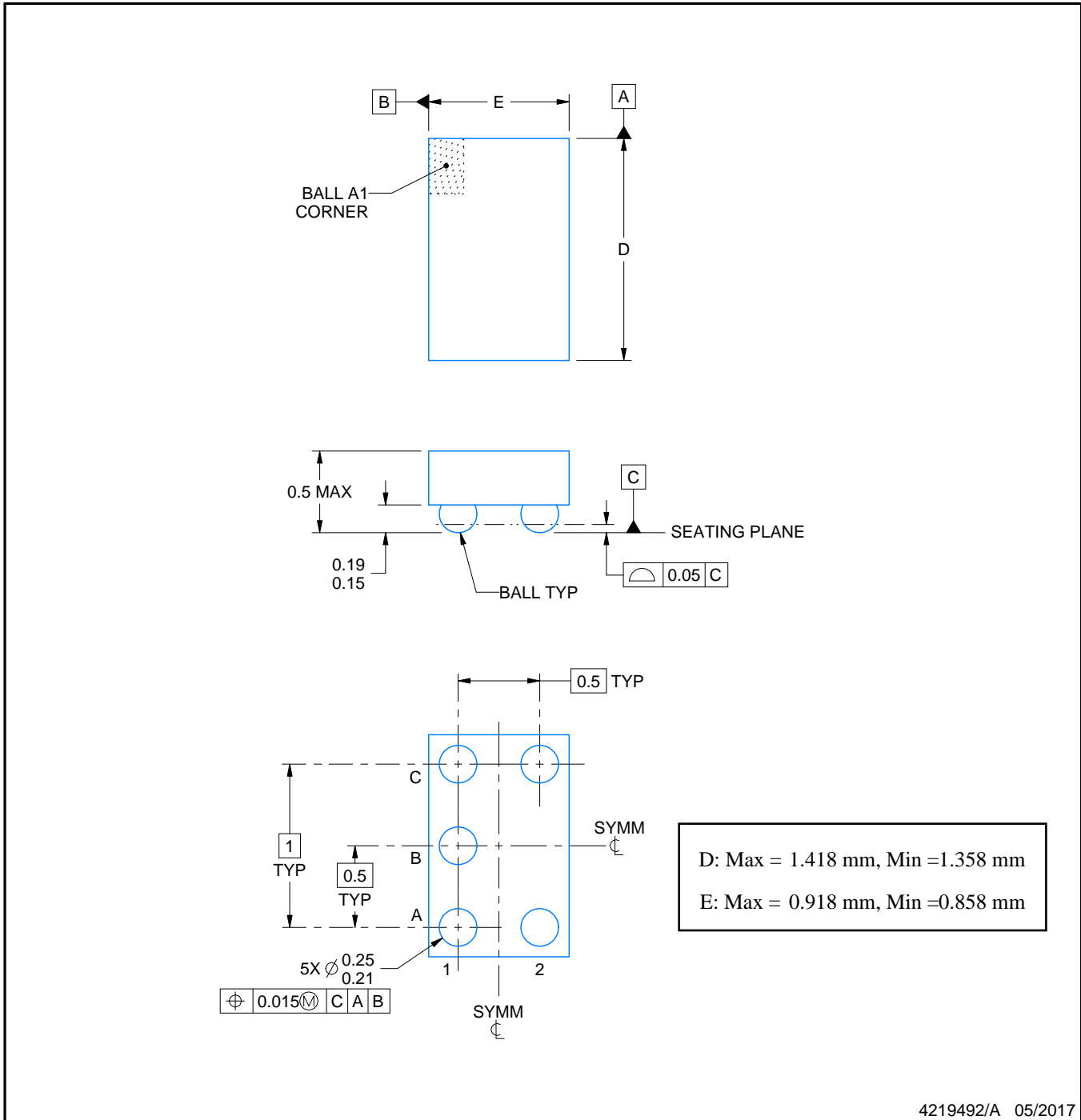
YZP0005



# PACKAGE OUTLINE

## DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS  
NOT TO SCALE

4219492/A 05/2017

NOTES: (continued)

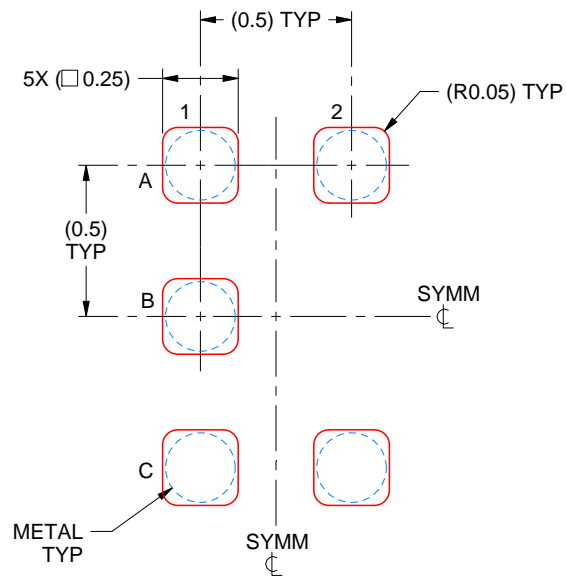
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YZP0005

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

4219492/A 05/2017

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



# EXAMPLE BOARD LAYOUT

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/G 03/2023

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

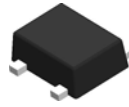
4214839/G 03/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



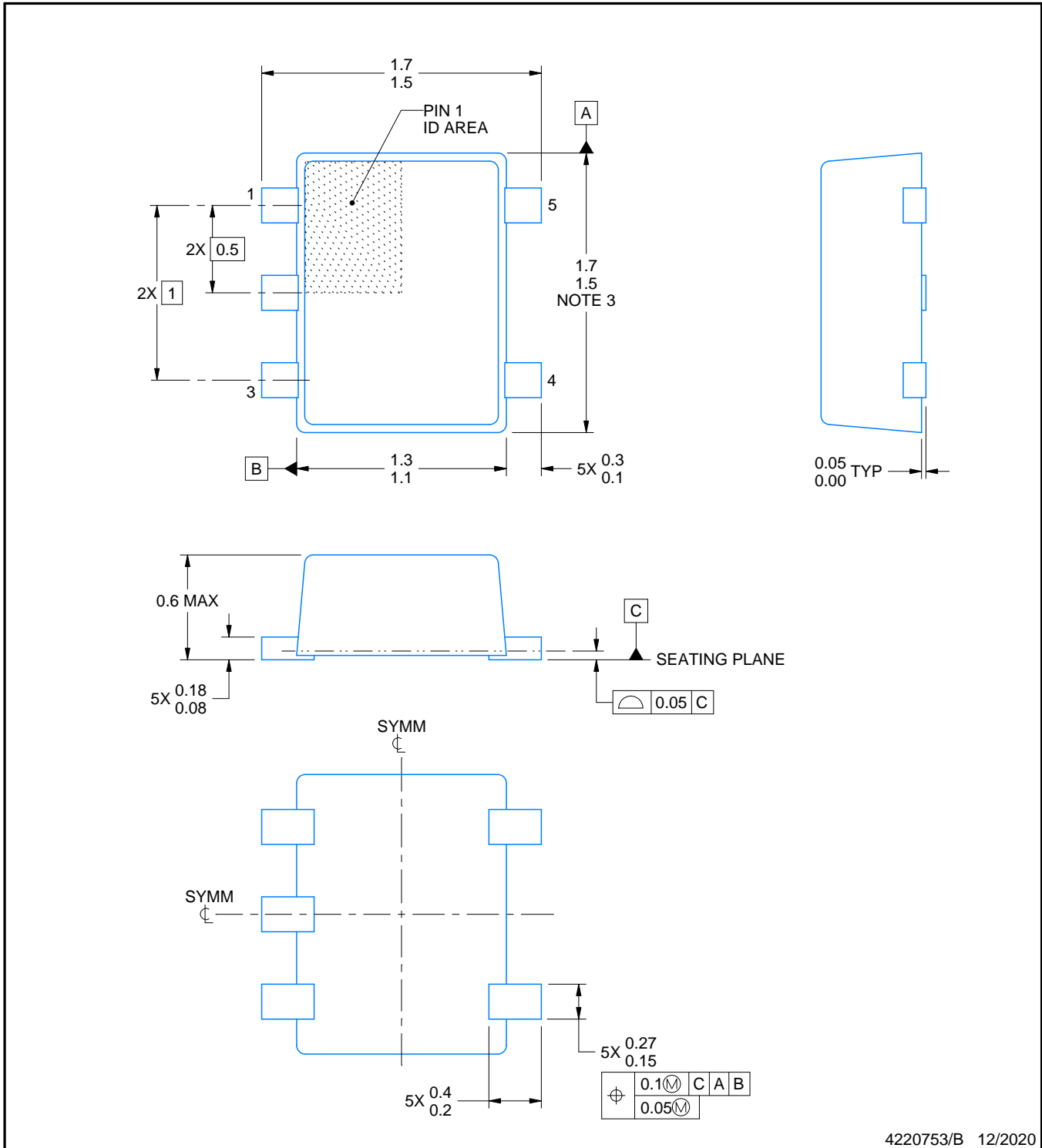
DRL0005A



# PACKAGE OUTLINE

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



4220753/B 12/2020

## NOTES:

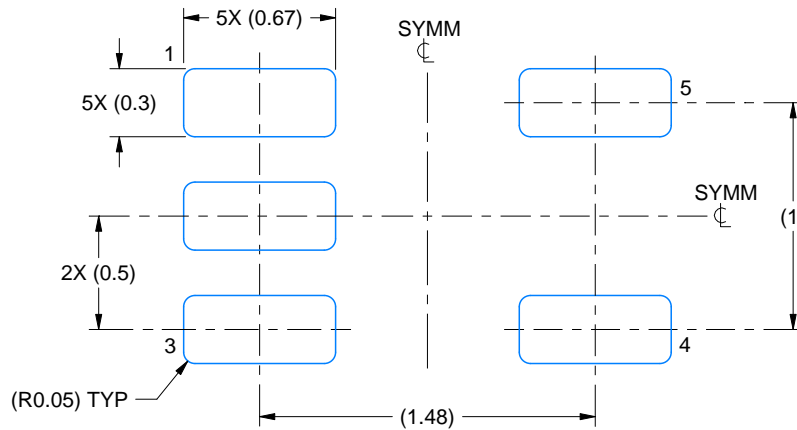
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-293 Variation UAAD-1

# EXAMPLE BOARD LAYOUT

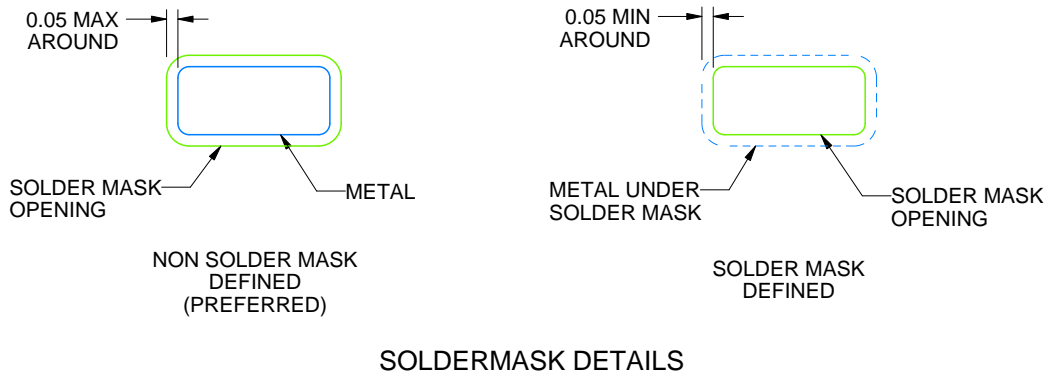
DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE  
SCALE:30X



SOLDERMASK DETAILS

4220753/B 12/2020

NOTES: (continued)

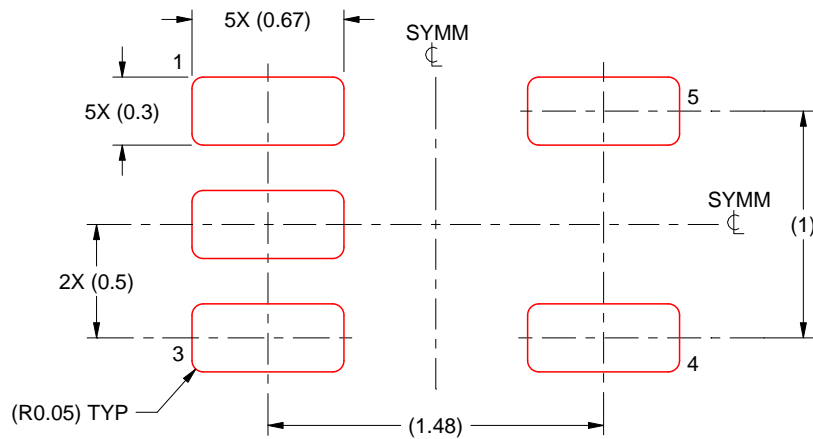
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DRL0005A

SOT - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:30X

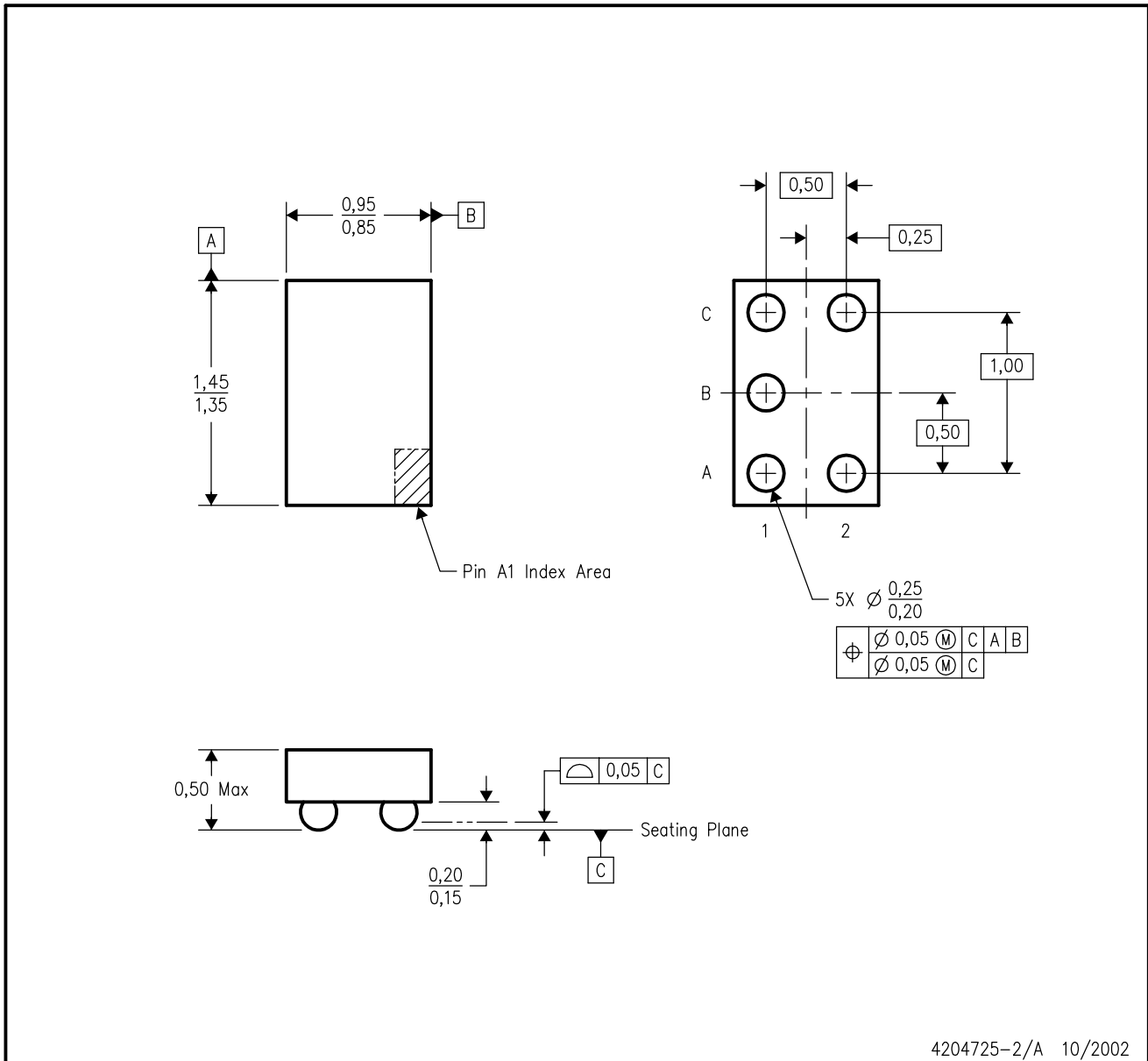
4220753/B 12/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

YEP (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY

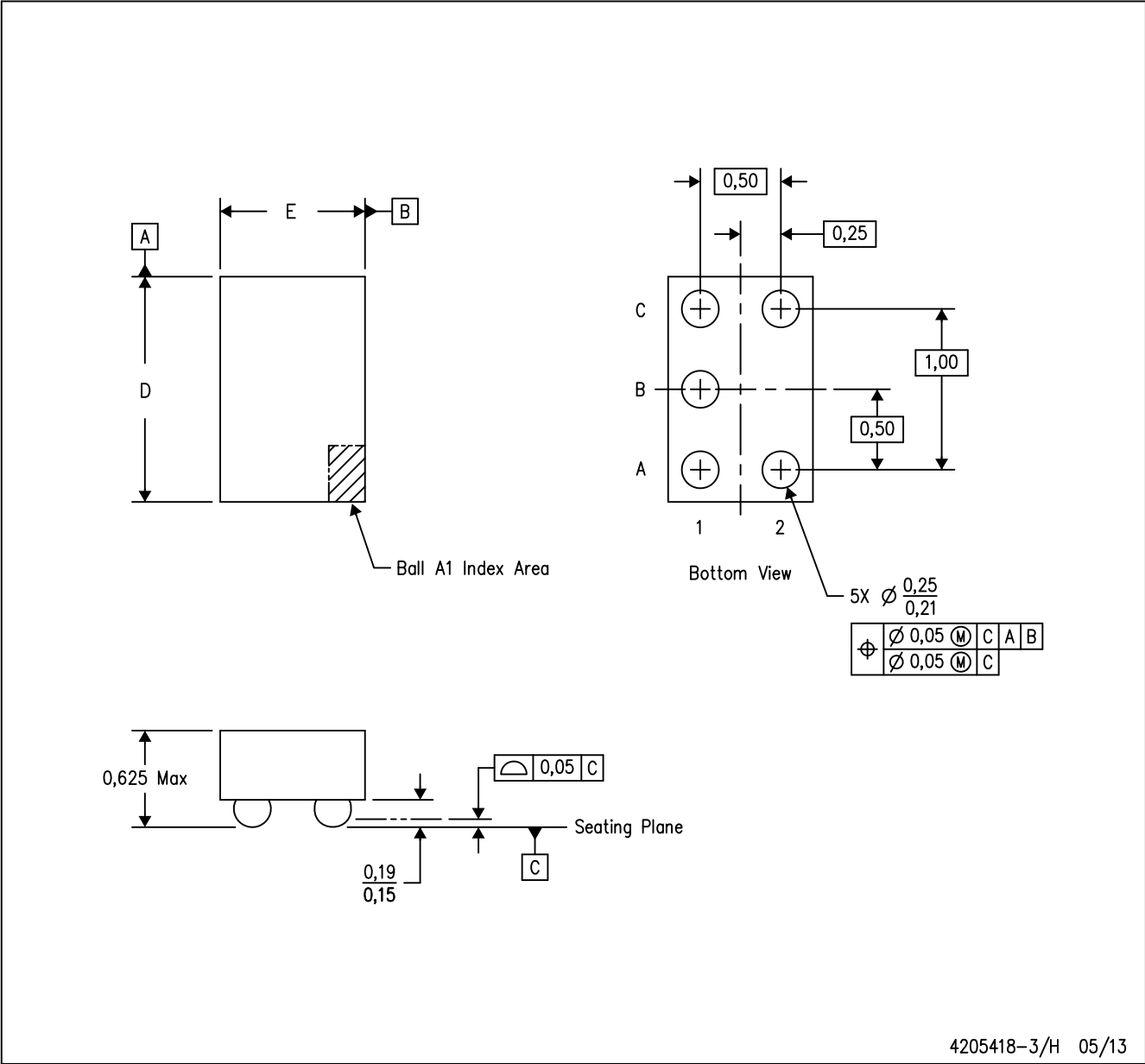


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. NanoStar™ package configuration.
  - D. This package is tin-lead (SnPb). Refer to the 5 YZP package (drawing 4204741) for lead-free.

NanoStar is a trademark of Texas Instruments.

YZT (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY

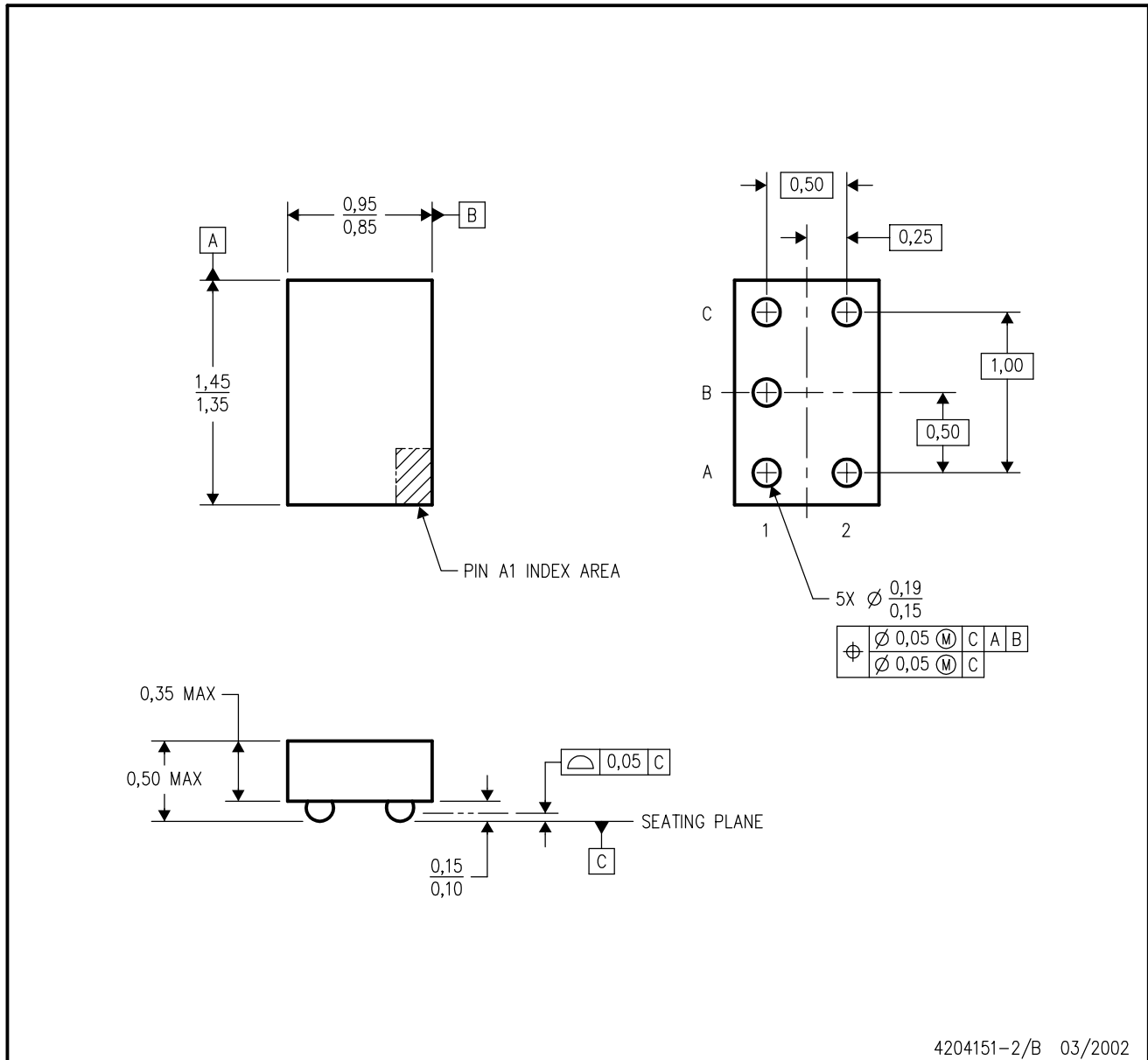


- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.

NanoFree is a trademark of Texas Instruments.

YZA (R-XBGA-N5)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. NanoFree™ package configuration.
  - D. Package complies to JEDEC MO-211 variation EA.
  - E. This package is lead-free. Refer to the 5 YEA package (drawing 4203167) for tin-lead (SnPb).

NanoFree is a trademark of Texas Instruments.

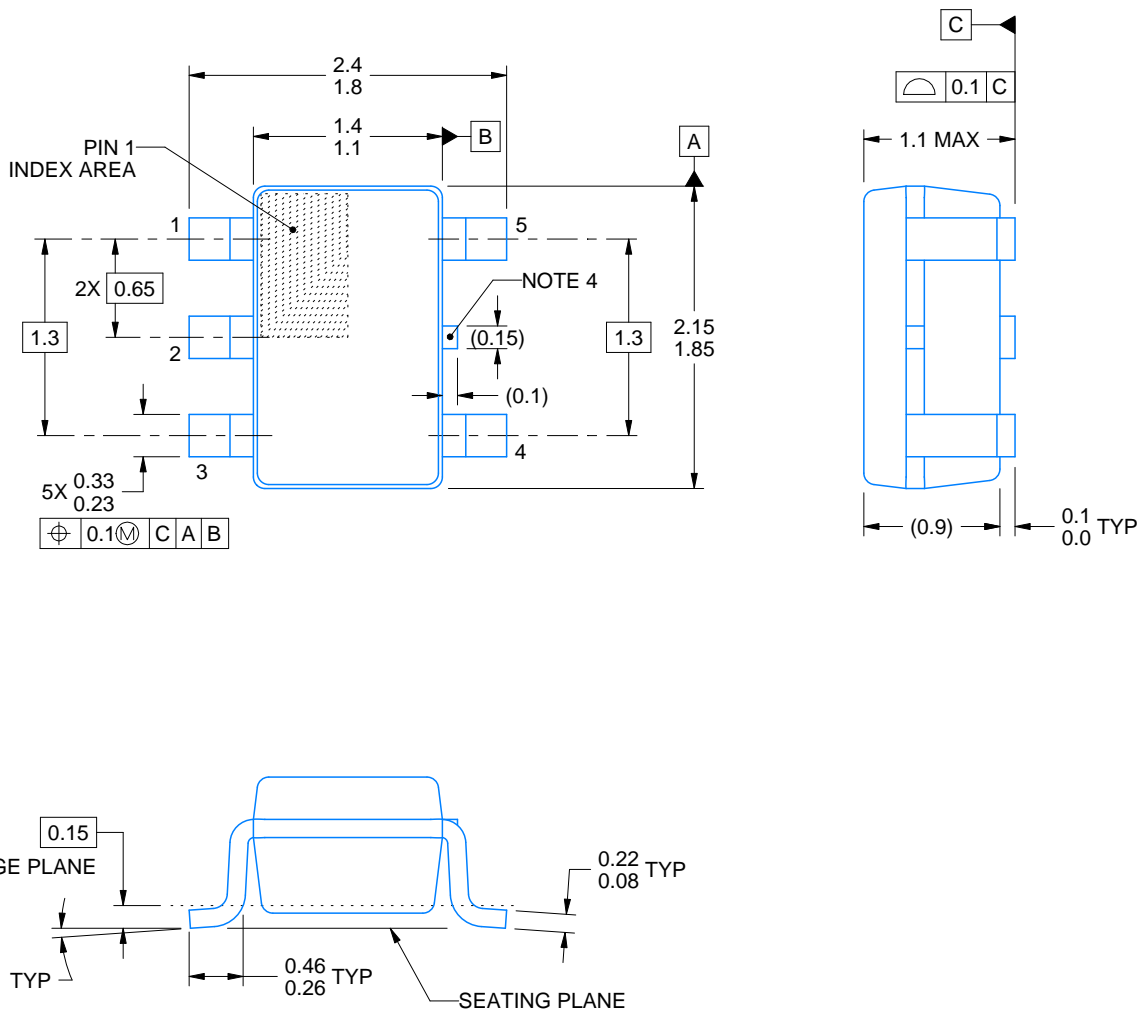
DCK0005A



# PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



4214834/C 03/2023

## NOTES:

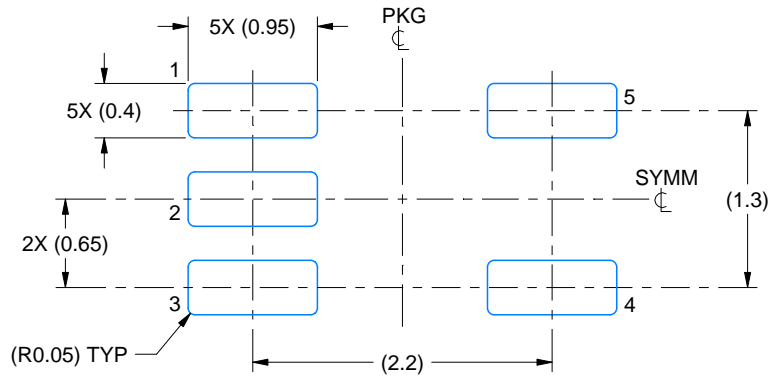
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.

# EXAMPLE BOARD LAYOUT

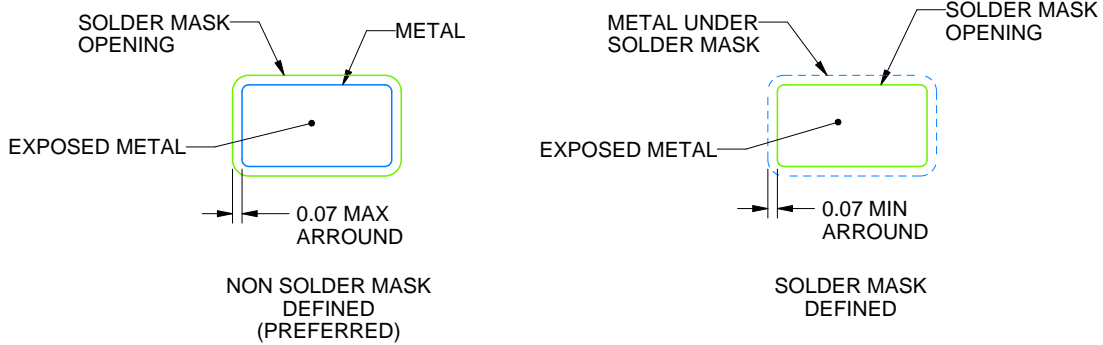
DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

4214834/C 03/2023

NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:18X

4214834/C 03/2023

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**DRY 6**

**USON - 0.6 mm max height**

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4207181/G



NOTES:

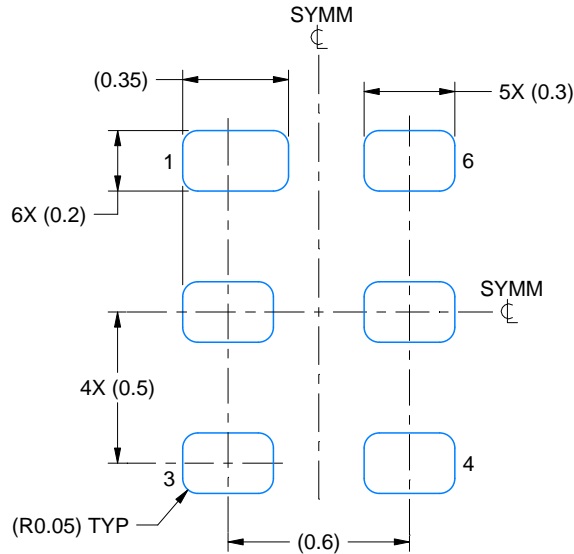
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

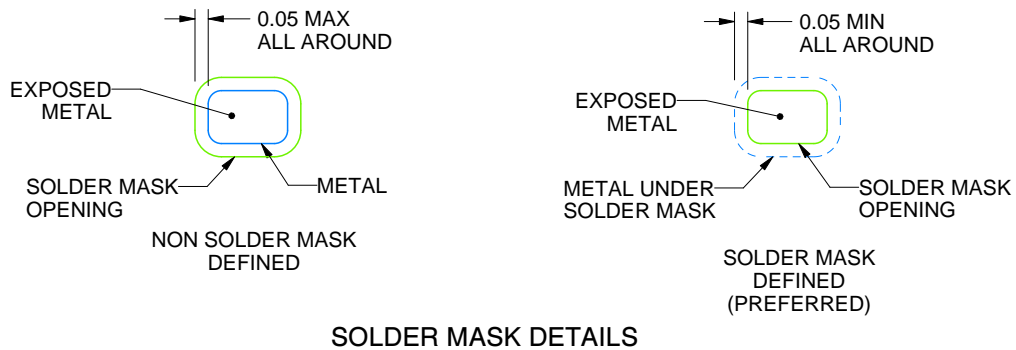
DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



**LAND PATTERN EXAMPLE**  
1:1 RATIO WITH PKG SOLDER PADS  
EXPOSED METAL SHOWN  
SCALE:40X



**SOLDER MASK DETAILS**

4222894/A 01/2018

NOTES: (continued)

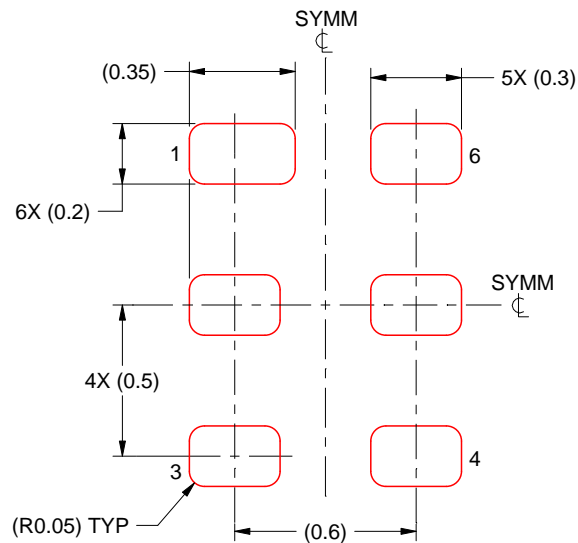
3. For more information, see QFN/SON PCB application report in literature No. SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).

# EXAMPLE STENCIL DESIGN

DRY0006A

USON - 0.6 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.075 - 0.1 mm THICK STENCIL  
SCALE:40X

4222894/A 01/2018

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

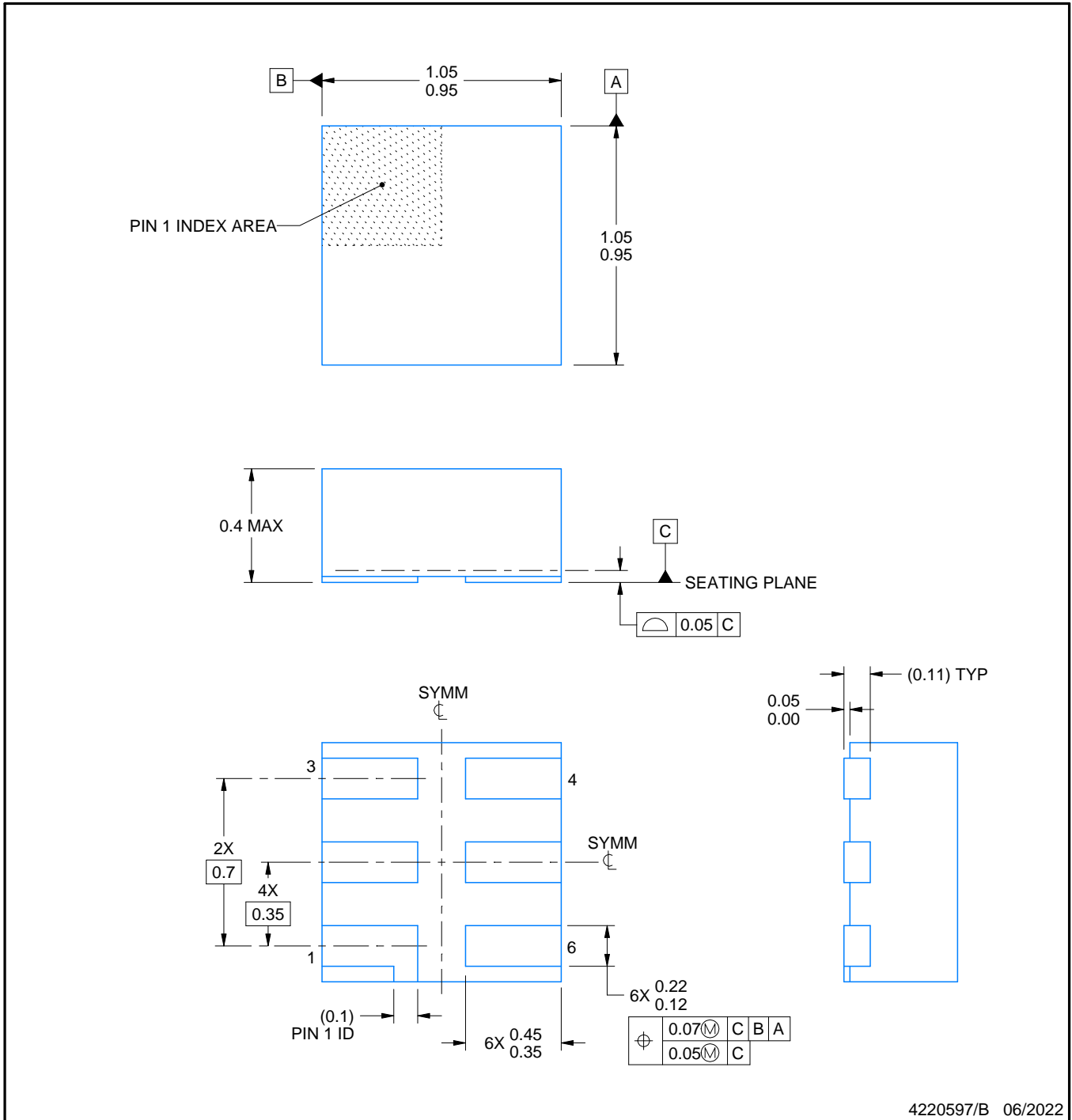


DSF0006A

# PACKAGE OUTLINE

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

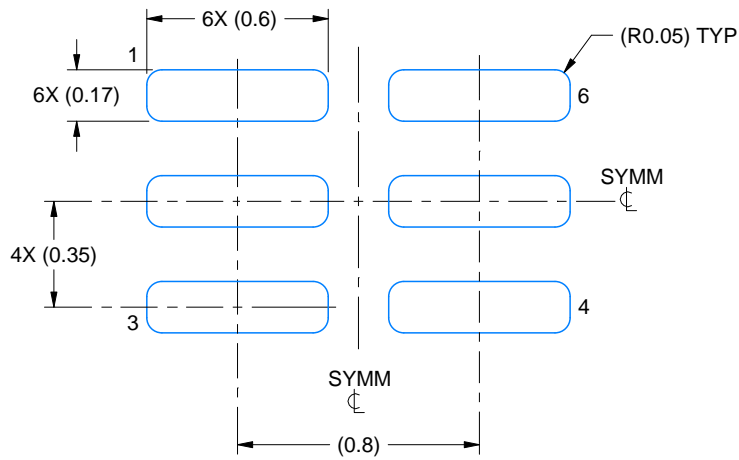
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MO-287, variation X2AAF.

# EXAMPLE BOARD LAYOUT

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:40X



SOLDER MASK DETAILS

4220597/B 06/2022

NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DSF0006A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.09 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:40X

4220597/B 06/2022

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



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