TPS7B69xx-Q1 高压超低 I_Q 低压降稳压器

1 特性

- 适用于汽车电子 应用
- 具有符合 AEC-Q100 的下列结果：
  - 器件温度 1 级：-40°C 至 125°C 的环境运行温度范围
  - 器件人体模型 (HBM) 静电放电 (ESD) 分类等级 2
  - 器件组件充电模式 (CDM) ESD 分类等级 C4B
- V_I 宽输入电压范围为 4V 至 40V，瞬态电压可达 45V
- 最大输出电流：150mA
- 低静态电流 (I_Q)：
  - 轻负载时典型值为 15µA
  - 整体温度范围下最大电流为 25µA
- 负载电流为 100mA 时，低压降电压典型值为 450mV
- 与低等效串联电阻 (ESR) 陶瓷输出电容（2.2 至 100µF）一起工作时保持稳定
- 固定输出电压选项为 2.5V、3.3V 和 5V
- 集成故障保护：
  - 热关断
  - 短路保护功能
- 封装：
  - 4 引脚小外形尺寸晶体管 (SOT)-223 封装
  - 5 引脚小外形尺寸晶体管 (SOT)-23 封装

2 应用范围

- 汽车
- 具有睡眠模式的信息娱乐系统
- 常开电池 应用
  - 车门模块
  - 遥控门锁系统
  - 发动机防盗系统

3 说明

TPS7B69xx-Q1 器件是一款低压降线性稳压器，其设计适用于高达 40V 的 V_I 操作。该器件在轻负载条件下的静态电流仅为 15µA（典型值），尤其适用于汽车应用中的待机微控制器 系统。

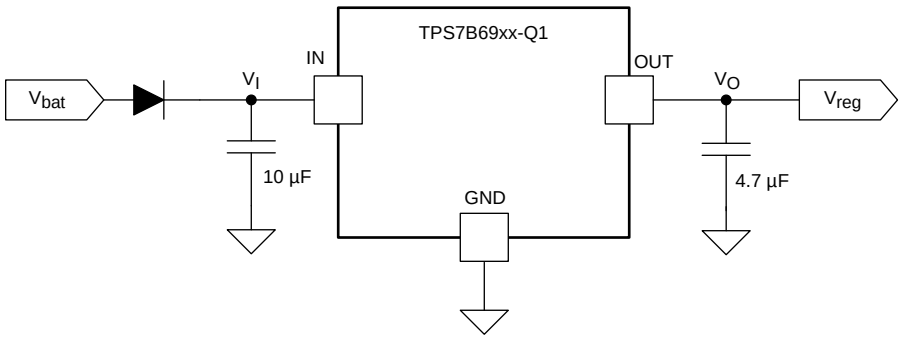
该器件具有集成短路保护和过流保护功能。TPS7B69xx-Q1 器件工作温度范围为 –40°C 至 125°C。凭借这些 特性，TPS7B6925-Q1、TPS7B6933-Q1 以及 TPS7B6950-Q1 器件非常适合在各种汽车应用的电源中 使用。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS7B6925-Q1 TPS7B6933-Q1 TPS7B6950-Q1	SOT-223 (4)	6.50mm x 3.50mm
	SOT-23 (5)	2.90mm x 1.60mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

4 典型应用电路原理图



目录

5 修订历史记录

Changes from Revision A (December 2014) to Revision B **Page**

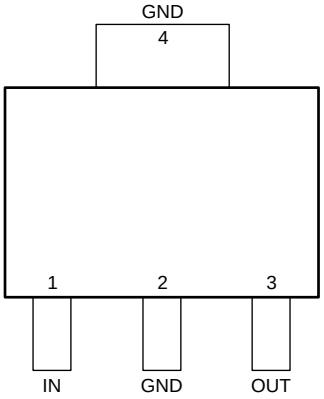
- 已更改 TPS7B6933-Q1 器件状态“*产品预览*”至“*量产数据*” ... 1
- 已添加 the TPS7B6933-Q1 device test results to the *Typical Characteristics* section ... 6

Changes from Original (November 2014) to Revision A **Page**

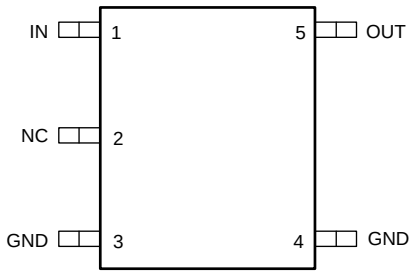
- 已更改 器件状态“*产品预览*”至“*量产数据*” ... 1

6 Pin Configuration and Functions

DCY Package
4-Pin SOT-223
Top View



DBV Package
5-Pin SOT-23
Top View



NC - No internal connection

Pin Functions

PIN			TYPE	DESCRIPTION
NAME	NO.			
	SOT-223	SOT-23		
GND	2	3	G	Ground reference
	4	4		
IN	1	1	P	Input power-supply voltage
NC	—	2	—	Not connected pin
OUT	3	5	P	Output voltage

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Unregulated input voltage	IN(2)(3)(4)	–0.3	45	V
Regulated output voltage	OUT(2)(3)	–0.3	7	V
Operating junction temperature range, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the GND terminal.
(3) Absolute negative voltage on these pins must not to go below –0.3 V.
(4) Absolute maximum voltage, withstands 45 V for 200 ms.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Other pins	±500	
			Corner pins (4 pin: 1, 3, and 4; 5 pin: 1, 3, 4, and 5)	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_I	Unregulated input voltage	4	40	V
V_O	Output voltage	0	5.5	V
C_O	Output capacitor requirements(1)	2.2	100	µF
ESR_{CO}	Output ESR requirements(2)	0.001	2	Ω
T_J	Operating junction temperature range	–40	150	°C

(1) The output capacitance range specified in this table is the effective value.
(2) Relevant ESR value at f = 10 kHz.

7.4 Thermal Information

THERMAL METRIC(1)(2)		DCY 4 PINS	DBV 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	64.2	210.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	46.8	126.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	13.3	38.4	
ψ_{JT}	Junction-to-top characterization parameter	6.3	16	
ψ_{JB}	Junction-to-board characterization parameter	13.2	37.5	

(1) The thermal data is based on the JEDEC standard high-K profile, JESD 51-7, 2s2p four layer board with 2-oz copper. The copper pad is soldered to the thermal land pattern. Also correct attachment procedure must be incorporated.
(2) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_{IN} = 14 V, 1 mΩ < ESR < 2 Ω, T_J = –40°C to 150 °C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (IN)						
V_I	Input voltage	Fixed 2.5-V output, I_O = 1 mA	4		40	V
		Fixed 3.3-V output, I_O = 1 mA	4		40	
		Fixed 5-V output, I_O = 1 mA	5.5		40	
I_Q	Quiescent current	Fixed 2.5-V and 3.3-V version, V_I = 4 to 40 V, Fixed 5-V version, V_I = 5.5 to 40 V, I_O = 0.2 mA		15	25	µA
$V_{IN(UVLO)}$	IN undervoltage detection	Ramp V_I up until the output turns on	3.65			V
		Ramp V_I down until the output turns OFF			3	
REGULATED OUTPUT (OUT)						
V_O	Regulated output	Fixed 2.5-V version, V_I = 4 to 40 V, I_O = 1 to 150 mA	–3%		3%	
		Fixed 3.3-V version, V_I = 5 to 40 V, I_O = 1 to 150 mA	–3%		3%	
		Fixed 5-V version, V_I = 6.5 to 40 V, I_O = 1 to 150 mA	–3%		3%	
$\Delta V_{O(\Delta VI)}$	Line regulation	V_I = 6 to 40 V, ΔV_O, I_O = 10 mA			10	mV
$\Delta V_{O(\Delta IL)}$	Load regulation	I_O = 1 to 150 mA, ΔV_O			20	mV
V_{DROP}	Dropout voltage	Fixed 2.5-V version, $V_I – V_O$, I_O = 50 mA			1.575	V
		Fixed 2.5-V version, $V_I – V_O$, I_O = 100 mA			1.575	
		Fixed 3.3-V version, $V_I – V_O$, I_O = 50 mA			799	mV
		Fixed 3.3-V version, $V_I – V_O$, I_O = 100 mA			800	
		Fixed 5-V version, $V_I – V_O$, I_O = 50 mA		220	400	
		Fixed 5-V version, $V_I – V_O$, I_O = 100 mA		450	800	
I_O	Output current	V_O in regulation	0		150	mA
I_{OCL}	Output current-limit	OUT short to ground	150		500	mA
PSRR	Power supply ripple rejection(1)	V_{rip} = 0.5 V_{pp}, Load = 10 mA, f = 100 Hz, C_O = 2.2 µF		60		dB
OPERATING TEMPERATURE RANGE						
T_{sd}	Junction shutdown temperature			175		°C
T_{hys}	Hysteresis of thermal shutdown			25		°C

(1) Design Information—Not tested, ensured by characterization.

7.6 Typical Characteristics

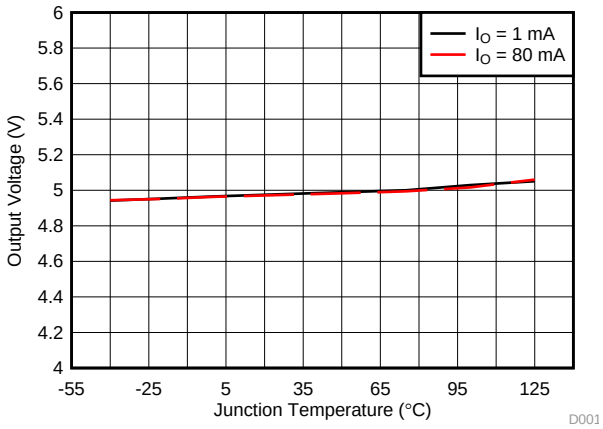


图 1. 5-V Output Voltage vs Junction Temperature

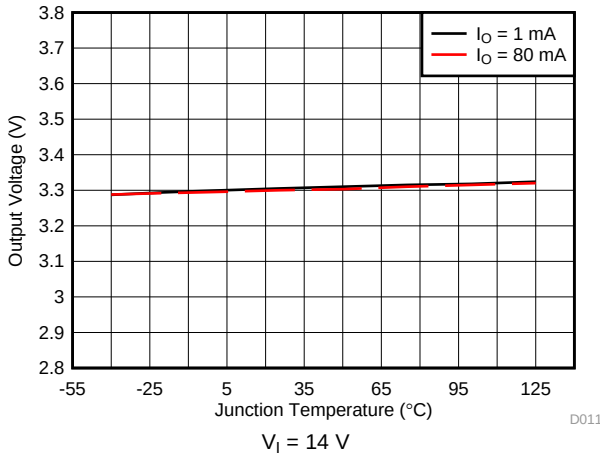


图 2. 3.3-V Output Voltage vs Junction Temperature

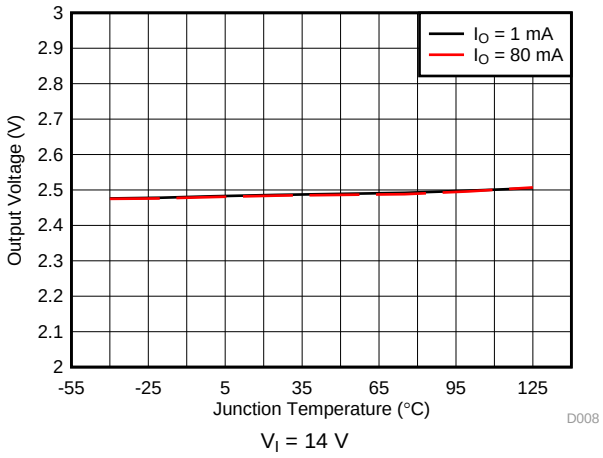


图 3. 2.5-V Output Voltage vs Junction Temperature

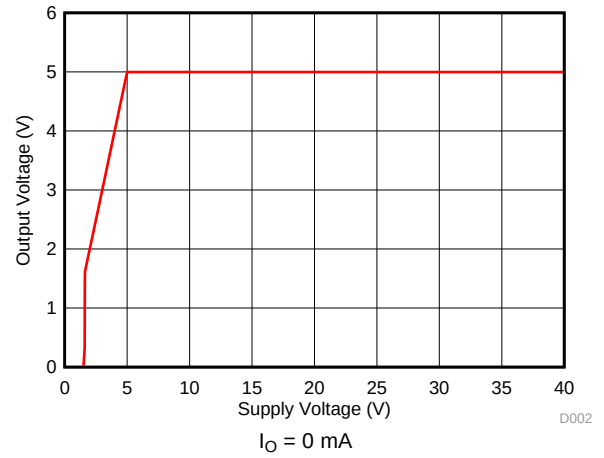


图 4. 5-V Output Voltage vs Supply Voltage

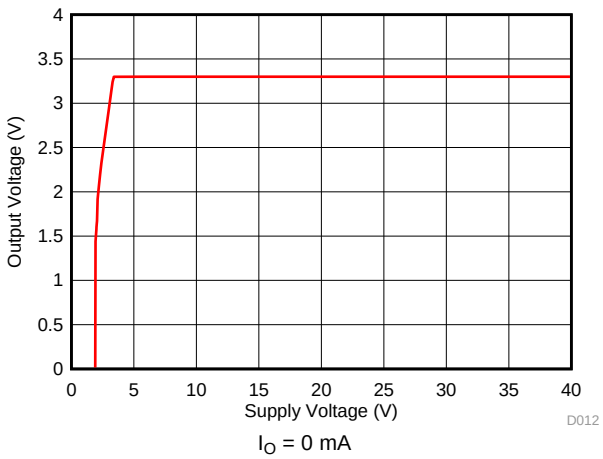


图 5. 3.3-V Output Voltage vs Supply Voltage

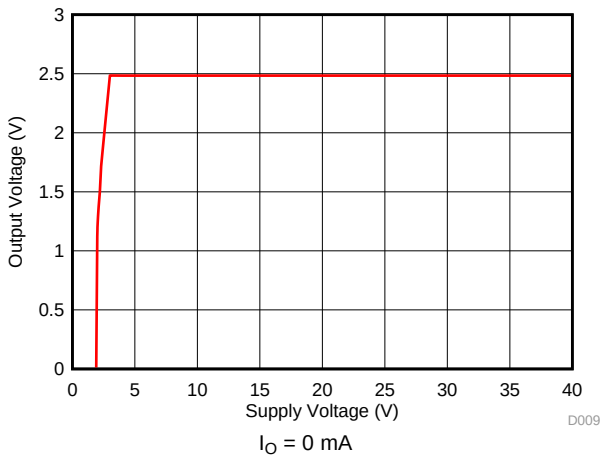


图 6. 2.5-V Output Voltage vs Supply Voltage

Typical Characteristics (接下页)

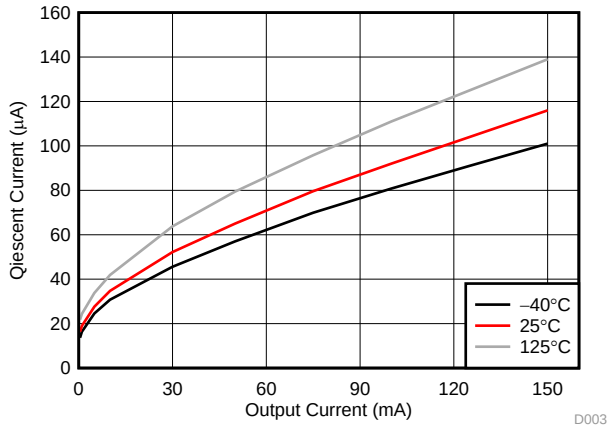
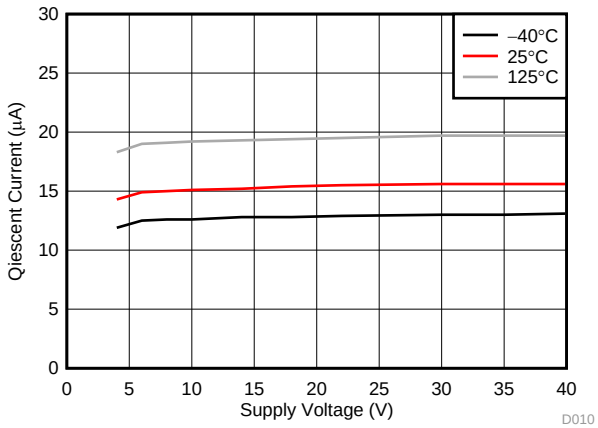


图 7. Quiescent Current vs Output Current



I_O = 0.2 mA

图 8. Quiescent Current vs Supply Voltage

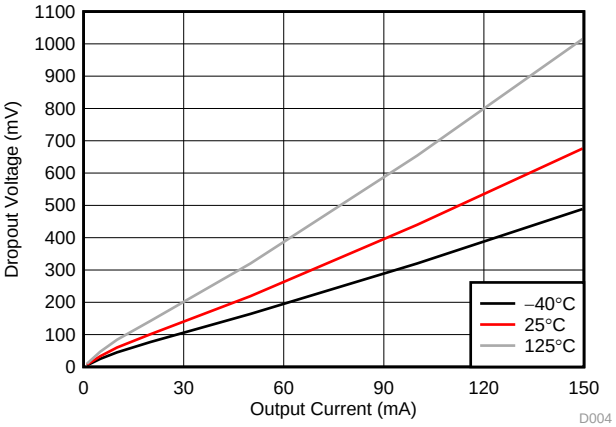
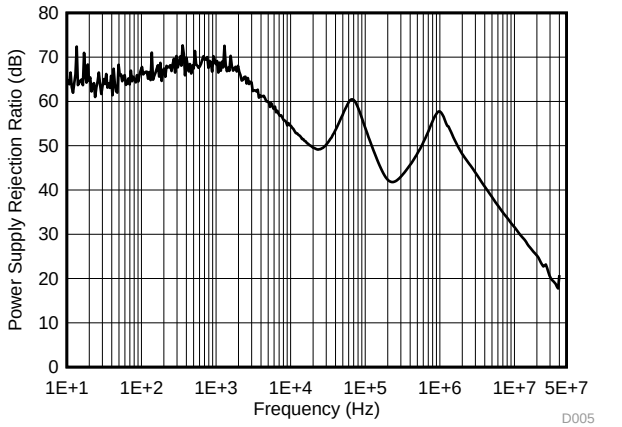
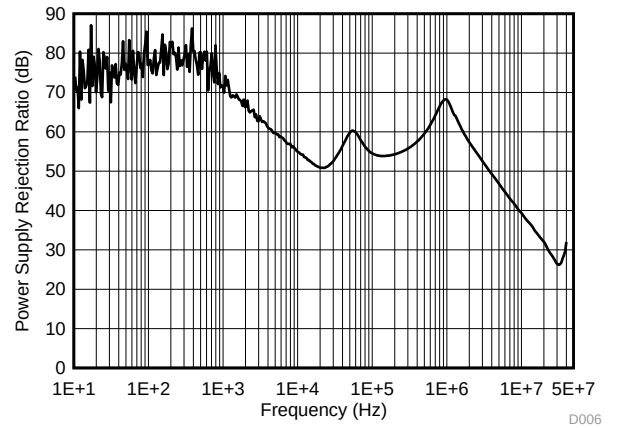


图 9. Dropout Voltage vs Output Current



I_O = 100 mA V_I = 14 V T_A = 25°C
C_O = 2.2 µF

图 10. Power Supply Rejection Ratio



I_O = 10 mA V_I = 14 V T_A = 25°C
C_O = 2.2 µF

图 11. Power Supply Rejection Ratio

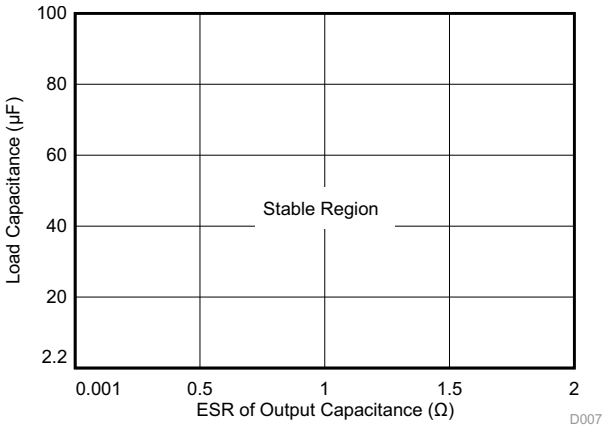


图 12. ESR Stability vs Output Capacitance

Typical Characteristics (接下页)

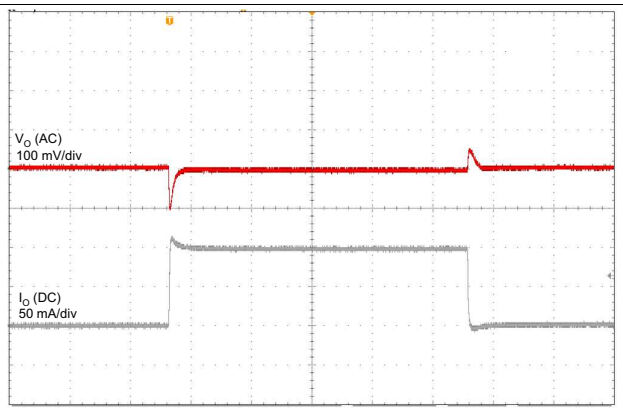


图 13. Load Transient (1 to 100 mA, 5 V)

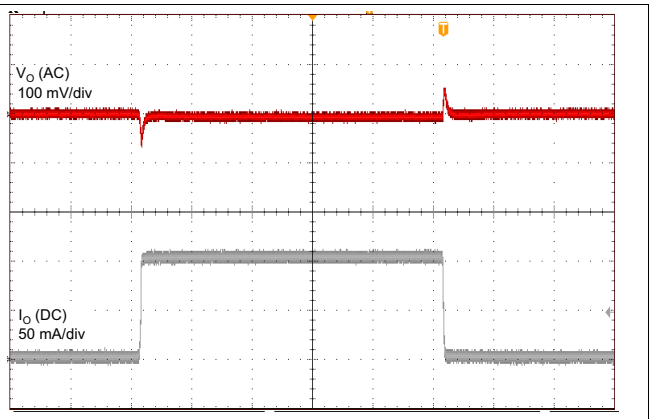


图 14. Load Transient (1 to 100 mA, 3.3 V)

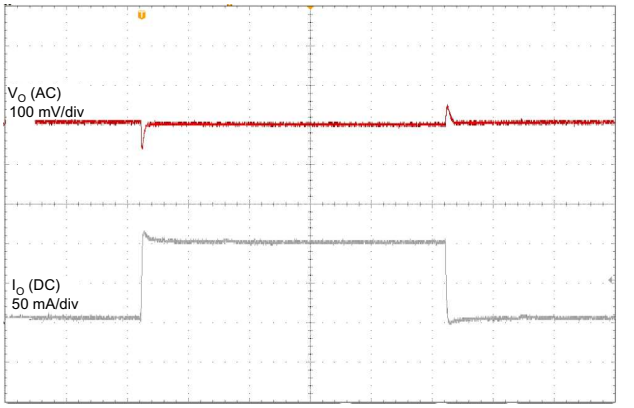


图 15. Load Transient (1 to 100 mA, 2.5 V)

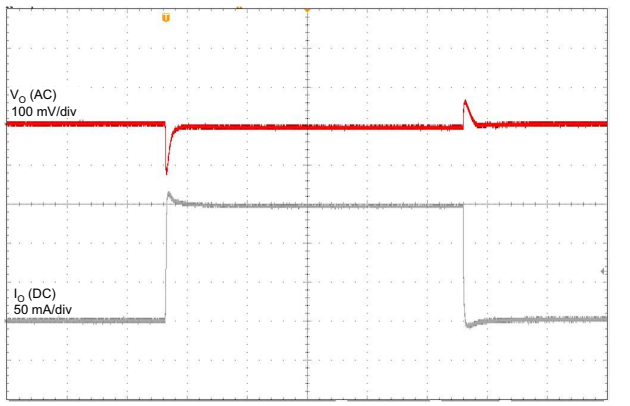


图 16. Load Transient (1 to 150 mA, 5 V)

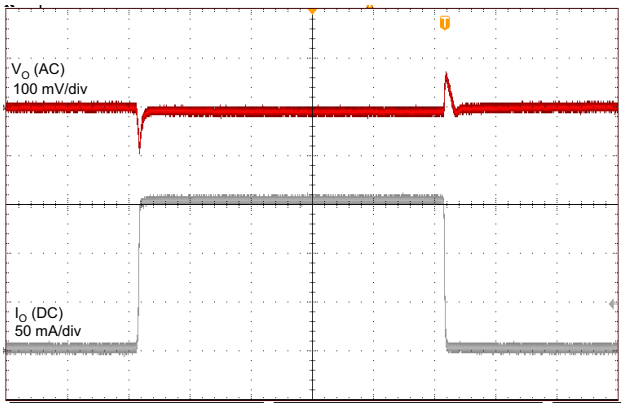


图 17. Load Transient (1 to 150 mA, 3.3 V)

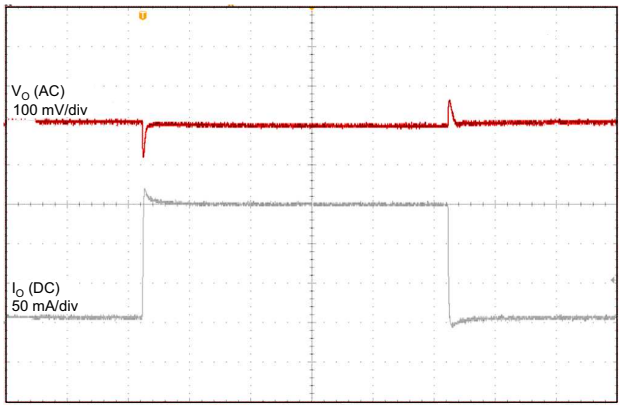


图 18. Load Transient (1 to 150 mA, 2.5 V)

Typical Characteristics (接下页)

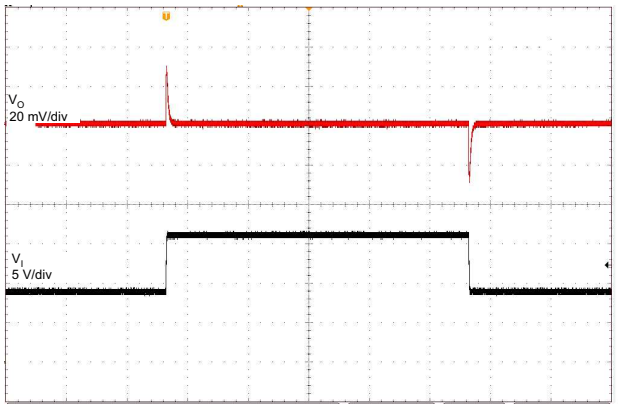


图 19. Line Transient (V_O = 5 V)

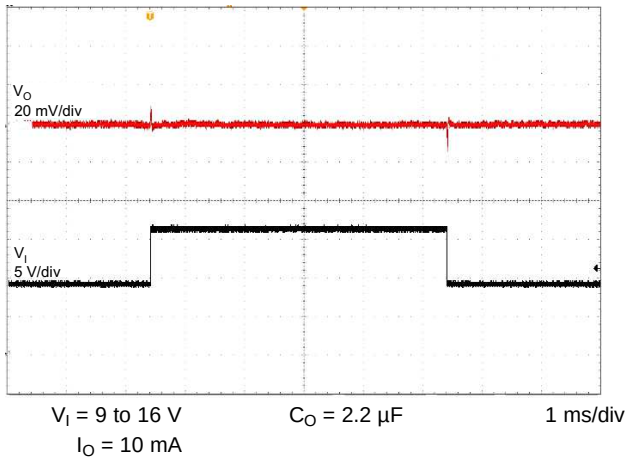


图 20. Line Transient (V_O = 3.3 V)

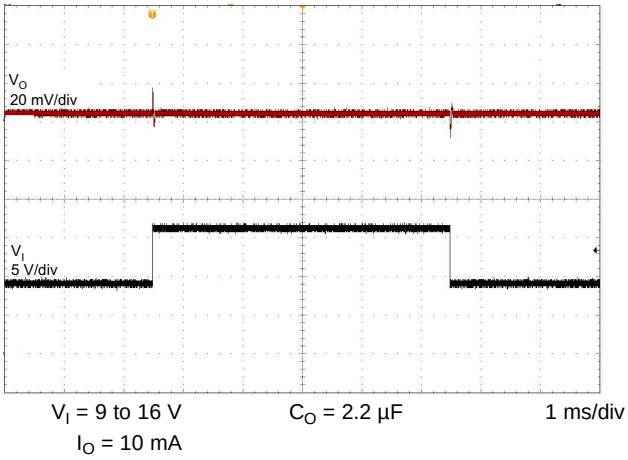


图 21. Line Transient (V_O = 2.5 V)

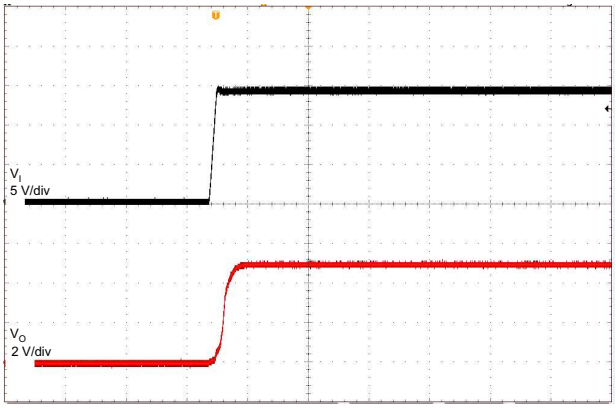


图 22. 5-V Power Up

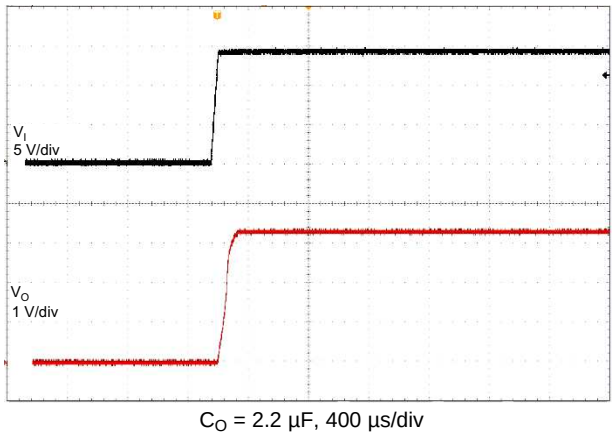


图 23. 3.3-V Power Up

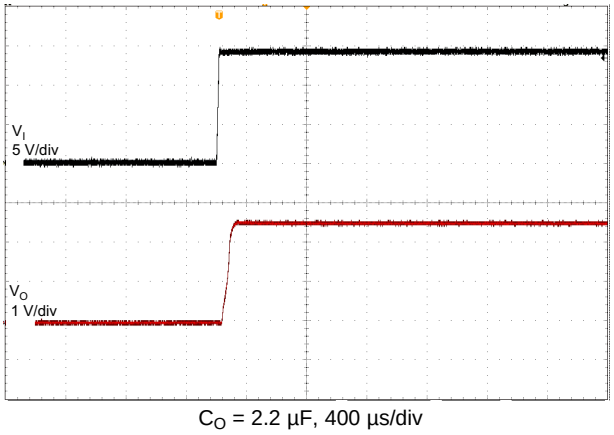


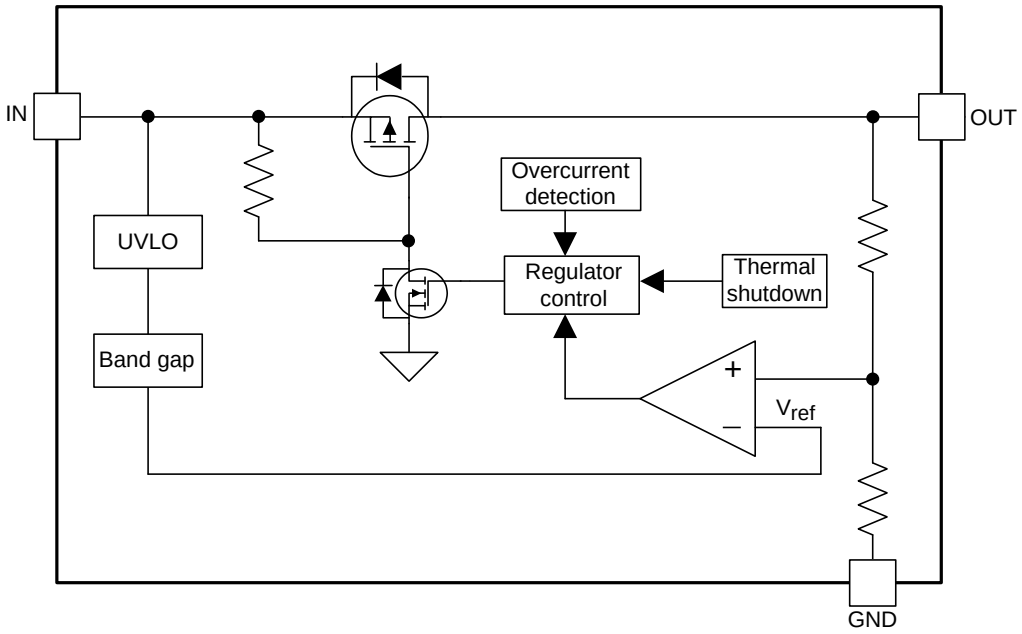
图 24. 2.5-V Power Up

8 Detailed Description

8.1 Overview

The TPS7B69xx-Q1 high-voltage linear regulator operates over a 4-V to 40-V input voltage range. The device has an output current capability of 150 mA and offers fixed output voltages of 2.5 V (TPS7B6925-Q1), 3.3 V (TPS7B6933-Q1) or 5 V (TPS7B6950-Q1). The device features a thermal shutdown and short-circuit protection to prevent damage during over-temperature and overcurrent conditions.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input (IN)

The IN pin is a high-voltage-tolerant pin. A capacitor with a value higher than 0.1 µF is recommended to be connected close to this pin to better the transient performance.

8.3.2 Output (OUT)

The OUT pin is the regulated output based on the required voltage. The output has current limitation. During the initial power up, the regulator has a soft start incorporated to control the initial current through the pass element and the output capacitor.

In the event that the regulator drops out of regulation, the output tracks the input minus a drop based on the load current. When the input voltage drops below the UVLO threshold, the regulator shuts down until the input voltage recovers above the minimum startup level.

8.3.3 Output Capacitor Selection

For stable operation over the full temperature range and with load currents up to 150 mA, use a capacitor with an effective value between 2.2 µF and 100 µF and ESR smaller than 2 Ω. To better the load transient performance, an output capacitor, such as a ceramic capacitor with low ESR, is recommended.

8.3.4 Low-Voltage Tracking

At low input voltages, the regulator drops out of regulation and the output voltage tracks input minus a voltage based on the load current (I_L) and switch resistor. This tracking allows for a smaller input capacitor and can possibly eliminate the need for a boost converter during cold-crank conditions.

Feature Description (接下页)

8.3.5 Thermal Shutdown

The TPS7B69xx-Q1 family of devices incorporates a thermal-shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature should not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature falls below the TSD trip point minus the hysteresis of TSD, the output turns on again. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

The purpose of the design of the internal protection circuitry of the TPS7B69xx-Q1 family of devices is for protection against overload conditions, not as a replacement for proper heat-sinking. Continuously running the TPS7B69xx-Q1 family of devices into thermal shutdown degrades device reliability.

8.4 Device Functional Modes

8.4.1 Operation With V_I Less Than 4 V

The TPS7B69xx-Q1 family of devices operates with input voltages above 4 V. The maximum UVLO voltage is 3 V and the device operates at an input voltage above 4 V. The device can also operate at lower input voltages; no minimum UVLO voltage is specified. At input voltages below the actual UVLO, the device shuts down.

8.4.2 Operation With V_I Greater Than 4 V

When V_I is greater than 4 V, if the input voltage is higher than V_O plus the dropout voltage, the output voltage is equal to the set value. Otherwise, the output voltage is equal to V_I minus the dropout voltage.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS7B69xx-Q1 family of devices is a 150-mA low-dropout linear regulator designed for up to 40-V V_I operation with only 15-µA quiescent current at light loads. Use the PSpice transient model to evaluate the base function of the device. To download the PSpice transient model, go to the device product folder on www.TI.com. In addition to this model, specific evaluation modules (EVM) are available for these devices. For the EVM and the EVM user guide, go to the device product folder.

9.2 Typical Application

图 25 shows the typical application circuit for the TPS7B69xx-Q1 family of devices. Based on the end-application, different values of external components can be used. An application can require a larger output capacitor during fast load steps to achieve better load transient response. TI recommends a low-ESR ceramic capacitor with a dielectric of type X5R or X7R for better load transient response.

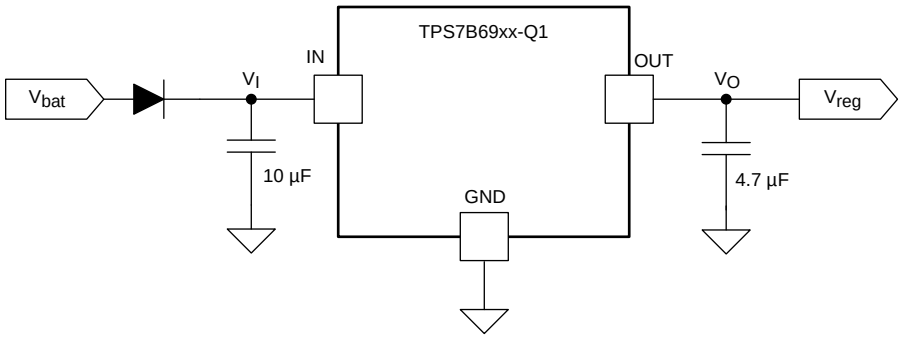


图 25. Typical Application Schematic for TPS7B69xx-Q1

9.2.1 Design Requirements

For this design example, use the parameters listed in 表 1.

表 1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUES
Input voltage range	4 to 40 V
Output voltage	2.5 V, 3.3 V, 5 V
Output current rating	150 mA
Output capacitor range	2.2 to 100 µF
Output capacitor ESR range	1 mΩ to 2 Ω

9.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
- Output Voltage
- Output current rating

9.2.2.1 Input Capacitor

The device requires an input decoupling capacitor, the value of which depends on the application. The typical recommend value for the decoupling capacitor is higher than 0.1 µF. The voltage rating must be greater than the maximum input voltage.

9.2.2.2 Output Capacitor

The device requires an output capacitor to stabilize the output voltage. The output capacitor value should be between 2.2 µF and 100 µF. The ESR value range should be between 1 mΩ and 2 Ω. TI recommends a ceramic capacitor with low ESR to improve the load transient response.

9.2.2.3 Power Dissipation and Thermal Considerations

Use 公式 1 to calculate the power dissipated in the device.

$$P_D = I_O \times (V_I - V_O) + I_Q \times V_I \quad (1)$$

where

- P_D = continuous power dissipation
- I_O = output current
- V_I = input voltage
- V_O = output voltage

Because I_Q « I_O, the term $I_Q \times V_I$ in 公式 1 can be ignored.

For a device under operation at a given ambient air temperature (T_A), use 公式 2 to calculate the junction temperature (T_J).

$$T_J = T_A + (Z_{\theta JA} \times P_D) \quad (2)$$

where

- $Z_{\theta JA}$ = junction-to-ambient air thermal impedance

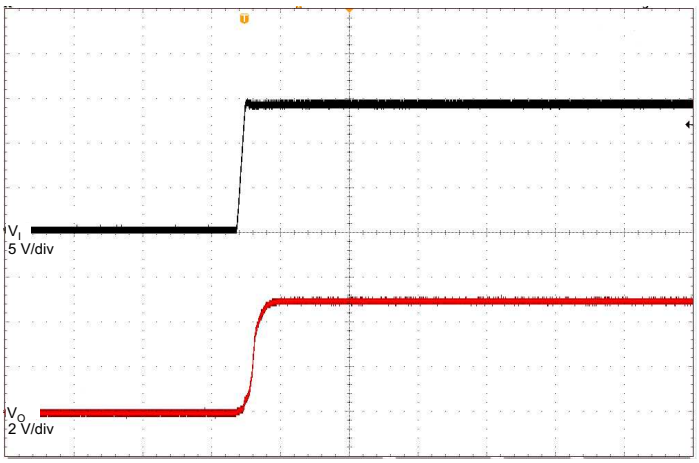
Use 公式 3 to calculate the rise in junction temperature because of power dissipation.

$$\Delta T = T_J - T_A = (Z_{\theta JA} \times P_D) \quad (3)$$

For a given maximum junction temperature (T_{Jmax}), use 公式 4 to calculate the maximum ambient air temperature (T_{Amax}) at which the device can operate.

$$T_{Amax} = T_{Jmax} - (Z_{\theta JA} \times P_D) \quad (4)$$

9.2.3 Application Curve



C_O = 2.2 µF, 400 µs/div

图 26. Power Up (5 V)

10 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range between 4 V and 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B69xx-Q1 device, TI recommends adding an electrolytic capacitor with a value of 10 µF and a ceramic bypass capacitor at the input.

11 Layout

11.1 Layout Guidelines

For the layout of TPS7B69xx-Q1 family of devices, place the input and output capacitors close to the devices as shown in 图 27 and 图 28. To enhance the thermal performance, TI recommends surrounding the device with some vias.

Minimize equivalent series inductance (ESL) and ESR to maximize performance and ensure stability. Place every capacitor as close as possible to the device and on the same side of the PCB as the regulator.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. TI strongly discourages the use of long traces because they can impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance specified in this product data sheet, use the same layout pattern used for the TPS7B69xx-Q1 evaluation board.

11.2 Layout Example

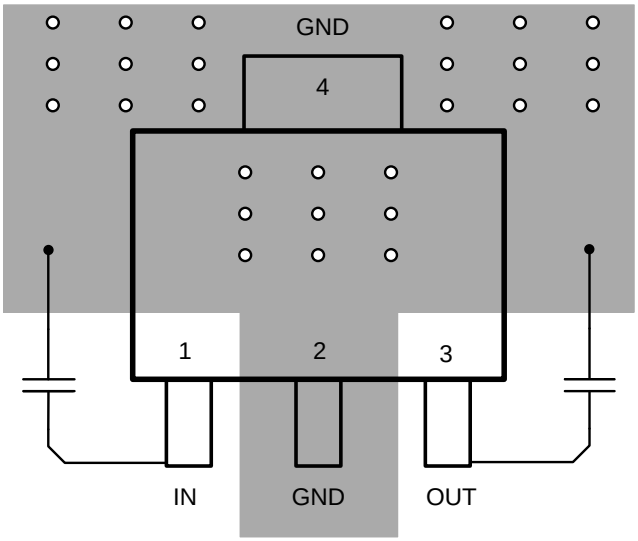


图 27. Layout Example for SOT-223 Package

Layout Example (接下页)

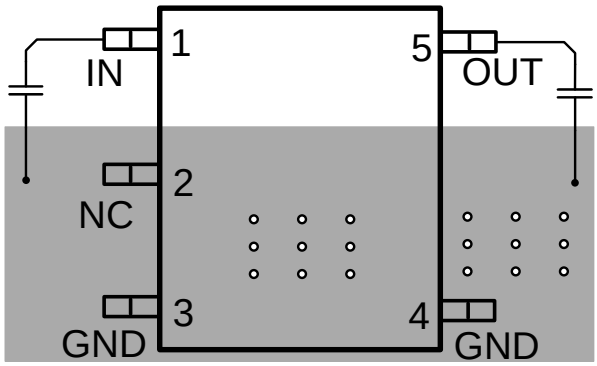


图 28. Layout Example for SOT-23 Package

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档如下：

《TPS7B6950EVM 用户指南》，SLVUAC0。

12.2 相关链接

下面的表格列出了快速访问链接。范围包括技术文档、支持和社区资源、工具和软件，以及样片或购买的快速访问。

表 2. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具与软件	支持与社区
TPS7B6925-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS7B6933-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处
TPS7B6950-Q1	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.3 商标

All trademarks are the property of their respective owners.

12.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7B6925QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	ZBE2	Samples
TPS7B6925QDCYRQ1	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	7B6925	Samples
TPS7B6933QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	ZBF2	Samples
TPS7B6933QDCYRQ1	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	7B6933	Samples
TPS7B6950QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1 YEAR	-40 to 125	ZAZ2	Samples
TPS7B6950QDCYRQ1	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 125	7B6950	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

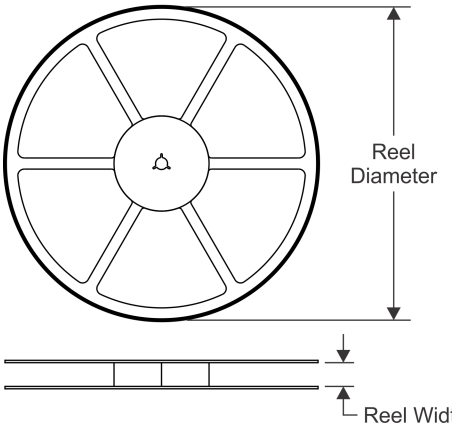
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

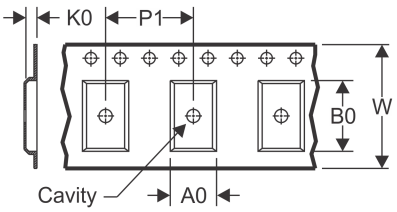
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

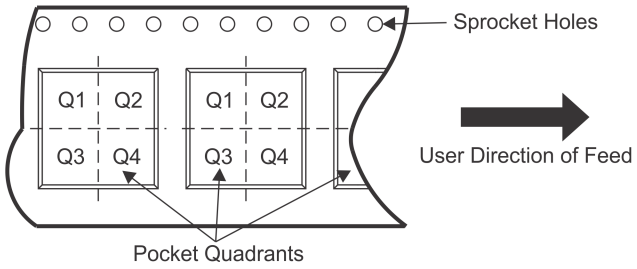


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

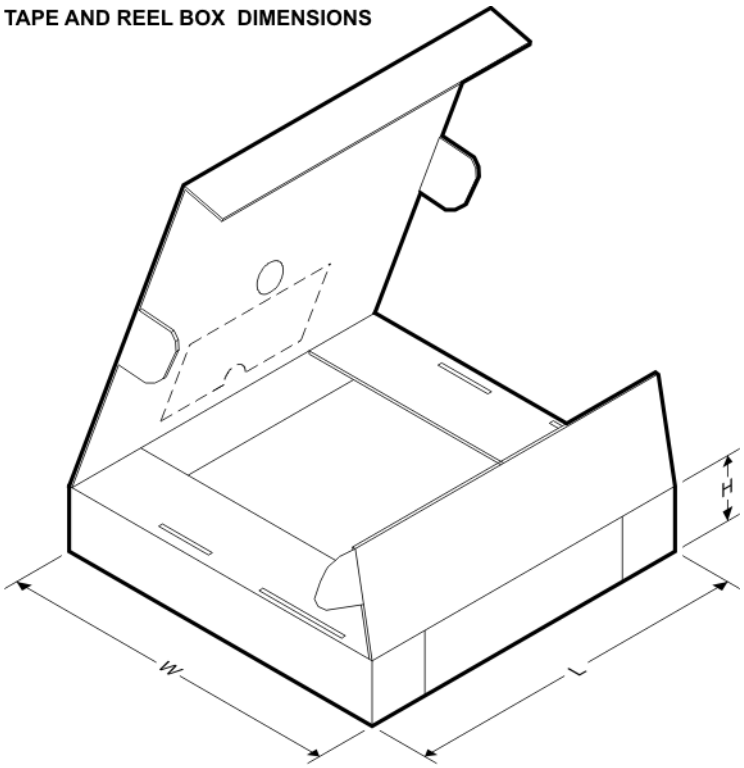
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B6925QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7B6925QDCYRQ1	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TPS7B6933QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7B6933QDCYRQ1	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3
TPS7B6950QDBVRQ1	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS7B6950QDCYRQ1	SOT-223	DCY	4	2500	330.0	12.4	7.05	7.4	1.9	8.0	12.0	Q3

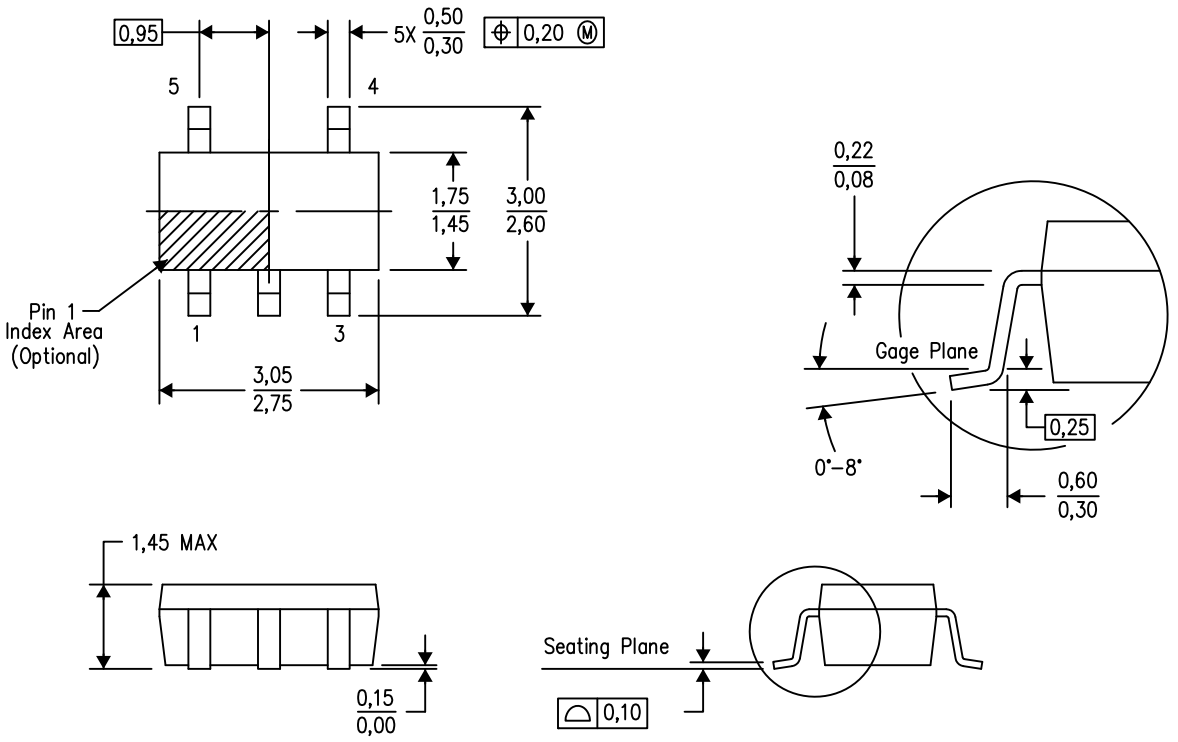
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B6925QDBVRQ1	SOT-23	DBV	5	3000	190.0	190.0	30.0
TPS7B6925QDCYRQ1	SOT-223	DCY	4	2500	340.0	340.0	38.0
TPS7B6933QDBVRQ1	SOT-23	DBV	5	3000	190.0	190.0	30.0
TPS7B6933QDCYRQ1	SOT-223	DCY	4	2500	340.0	340.0	38.0
TPS7B6950QDBVRQ1	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS7B6950QDCYRQ1	SOT-223	DCY	4	2500	340.0	340.0	38.0

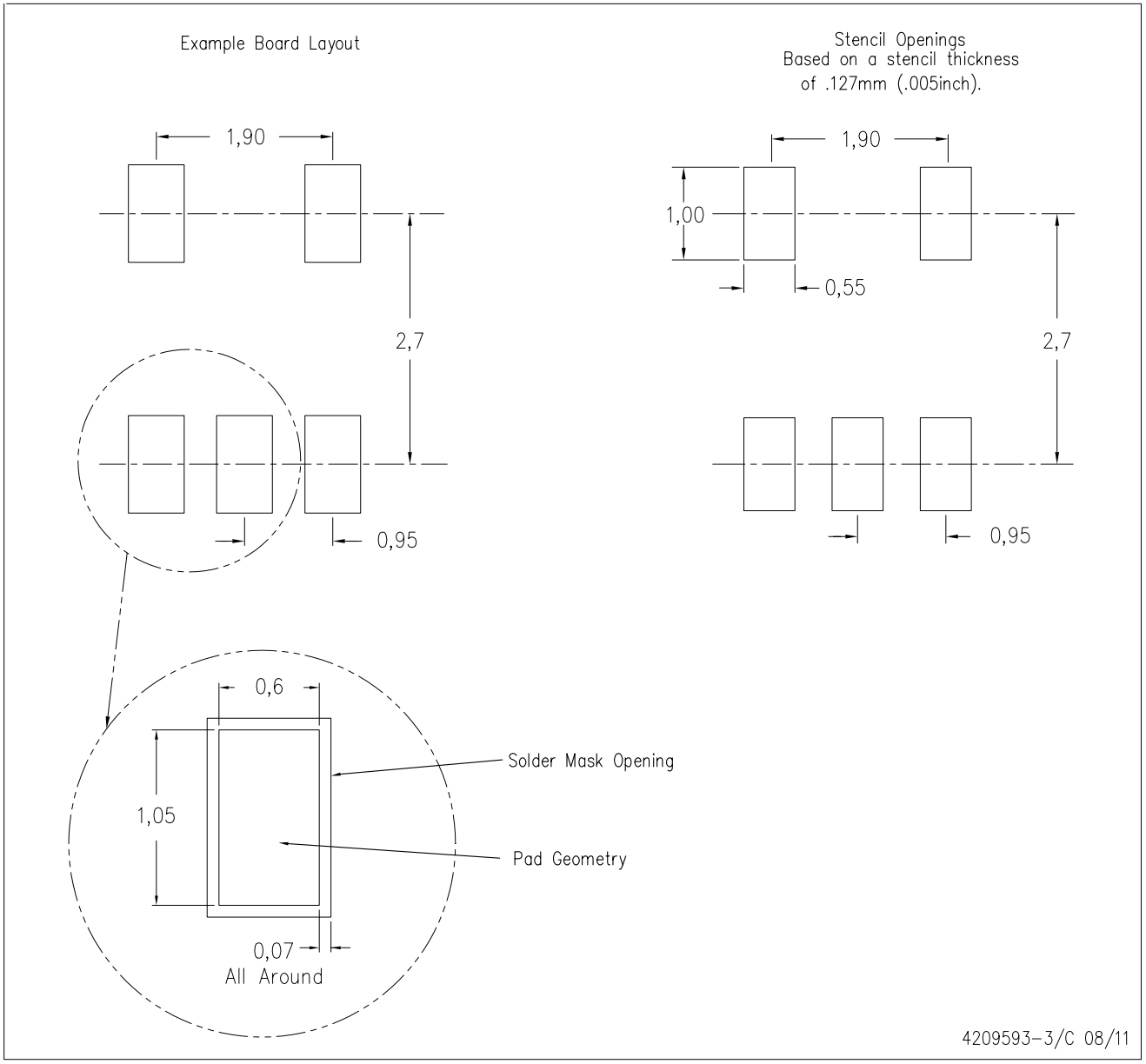
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

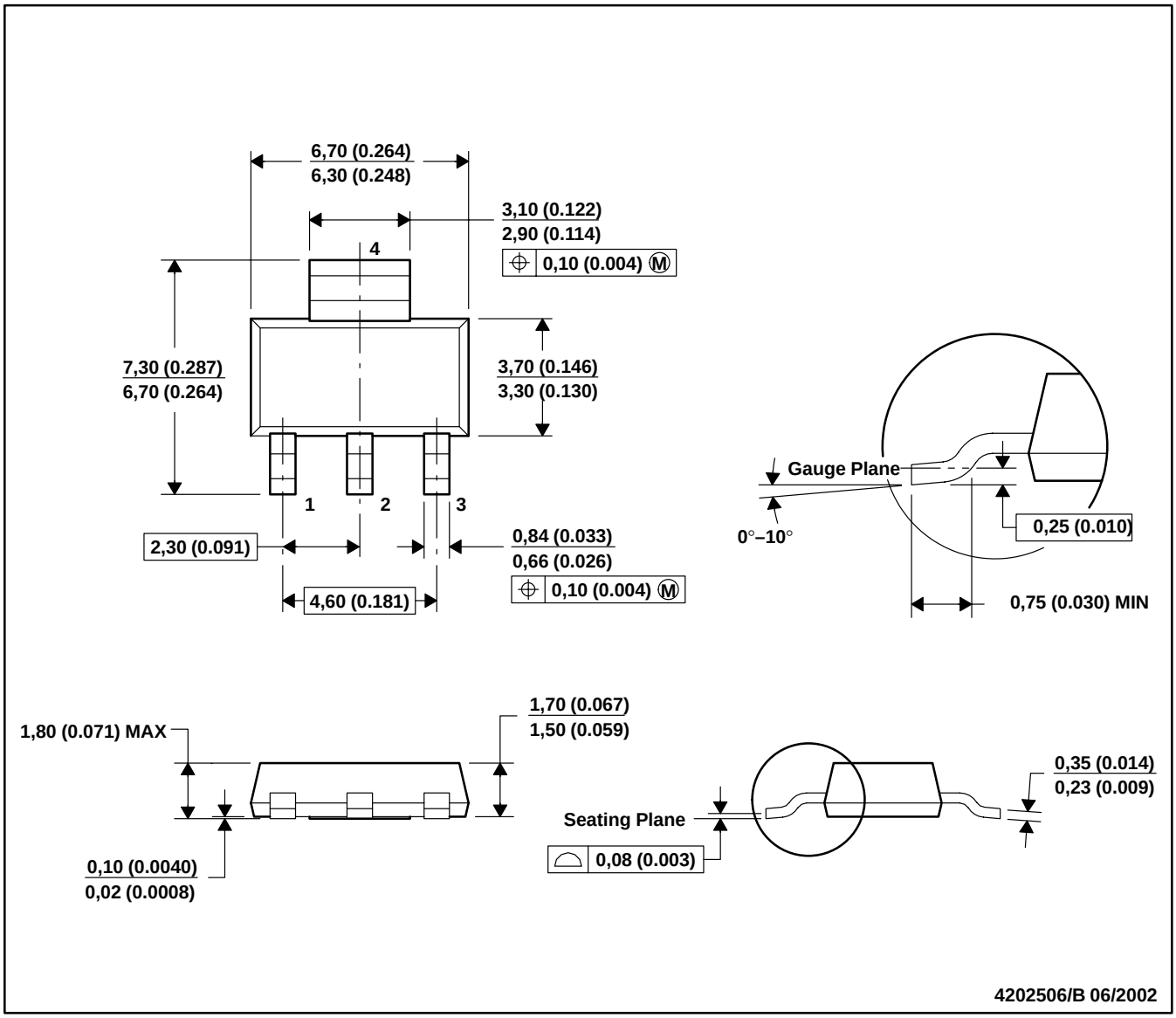
DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

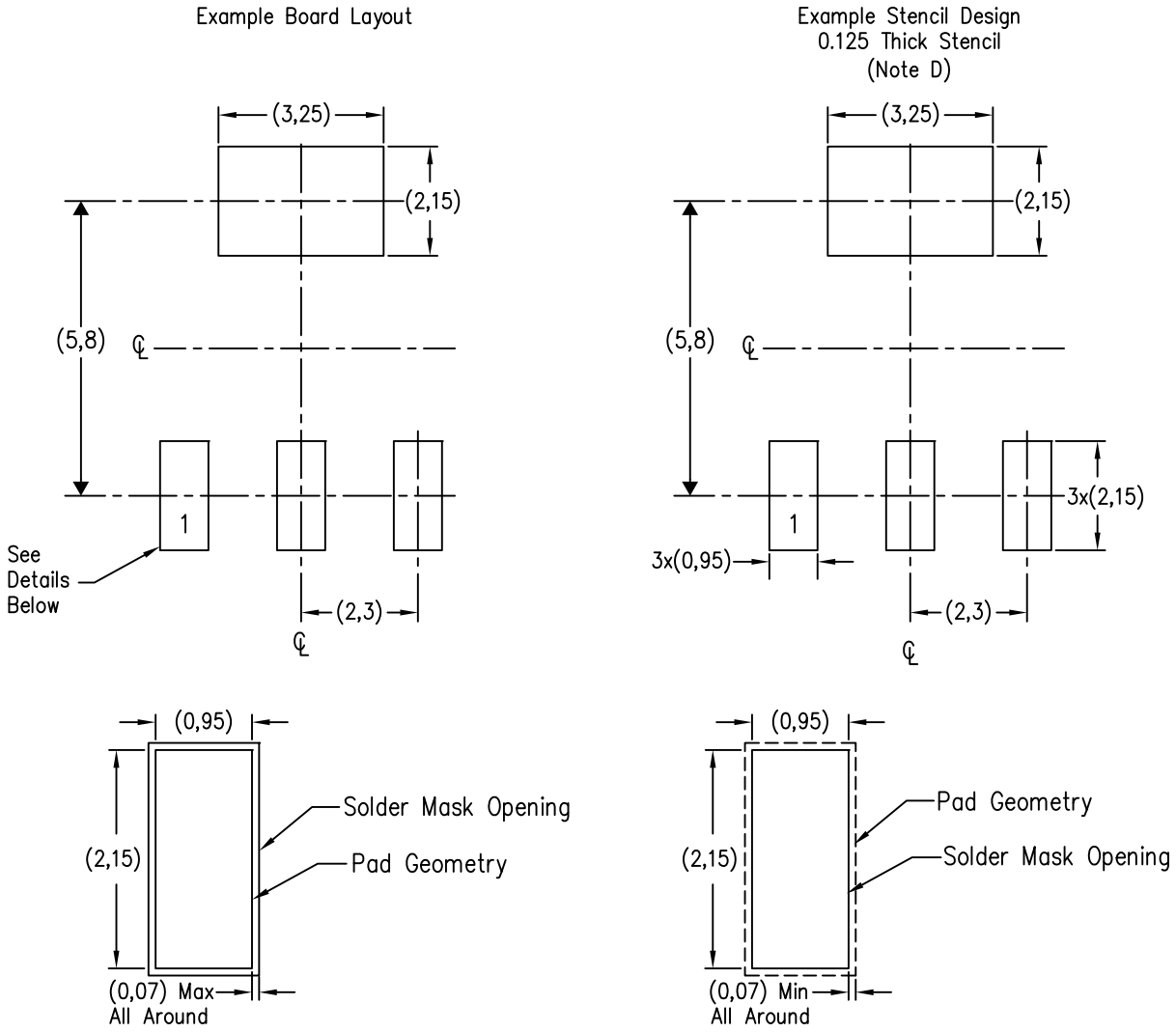
MPDS094A – APRIL 2001 – REVISED JUNE 2002

DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**



NOTES: A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC TO-261 Variation AA.

DCY (R–PDSO–G4) PLASTIC SMALL OUTLINE



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil recommendations. Refer to IPC 7525 for stencil design considerations.

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